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DEVICE PROCESS PHYSICS

Andris Ezis

Universal Energy Systems, Inc.
4401 Dayton-Xenia Road
Dayton, OH 45432

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MICHAEL J. PAULUS, 1LT
Project Engineer

EDWIN B. CHAMPAGNE, Actg Chief
Electronic Research Branch

FOR THE COMMANDER

WILLIAM J. EDWARDS, Director
Electronic Technology Division
Avionics Laboratory

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The objective of this program involved (a) the evaluation of the operational limits of Modulation Doped Field Effect Transistors (MODFETs) and (b) the development of a Bipolar Inversion Channel Field Effect Transistor (BICFET) for high speed applications. In the first part of the program, investigations were carried out on AlGaAs/GaAs MODFET isolation and contact structure and stability. Conventional and self-aligned gate MODFET fabrication processes were developed using both mesa and planar isclation technology. A comprehensive test pattern mask set was designed and fabricated for device and material parameter characterization. Backgating measurements were carried out for backgate-MODFET spacings ranging from 2 to 40 μm for various material and device structures. Conventional furnace and transient annealed Au/Ge/Ni ohmic contacts were investigated using both analytical and electrical characterization techniques. The second part of the program involved development of theory and fabrication process technology of a BICFET,

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One-dimensional semi-analytical and finite difference numerical simulations were carried out to determine the dc electrical characteristics and space charge distributions of BICFETs based on the AlGaAs/GaAs heterostructure. A basic BICFET test pattern mask set was designed and fabricated and preliminary process development was carried out.

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SECTION I
INTRODUCTION

The development of advanced electronic systems, which are capable of operating at high frequencies, has placed a demand on the development of new generations of high speed electronic devices. The effective implementation of these devices requires a knowledge of their extrinsic operational limits which may be based on the physics and chemistry of the particular materials structure or on the fabrication process. The Modulation Doped Field Effect Transistor (MODFET) is an attractive candidate for high frequency digital and analog systems due to its demonstrated high speed, low power and low noise performance. In the first part of the program, investigations were carried out on the MODFET in the areas of device isolation, contact structure and stability. The main advantage of the MODFET compared with the conventional GaAs MESFET is that part of the channel consists of a high mobility two-dimensional electron gas (2DEG) which lies at the heterojunction of two semiconductors of dissimilar band gap energies. The close confinement of the high charge density 2DEG to the gate allows the MODFET to exhibit high transconductances. In this program, n-type MODFETs based on the $Al_{0.3}Ga_{0.7}As$/GaAs heretrostructure were studied. For this material combination, the electron gas, supplied by ionized donor atoms in the AlGaAs, lies in the undoped high purity GaAs layer.

In the initial phase of the MODFET investigations, work was carried out on conventional and self-aligned gate MODFET fabrication process development. A comprehensive test pattern mask set was designed and fabricated in order to conduct investigations on MODFET isolation and contact and heterostructure material stability. The magnitude and mechanism of backgating in MODFETs were investigated as a function of device and MBE material structure for both mesa and planar isolated structures. The structure of contacts fabricated by both conventional and transient anneal processing was analyzed by transmission electron microscopy, energy dispersive X-ray analysis, and Auger spectroscopy techniques. The effects of stressing on the electrical properties of the low resistance contacts were studied and compared with the contact structure.

The work carried out in this program on MODFET fabrication process development and device characterization is described in Section 2. MODFET isolation investigations are described in Section 3 and MODFET contact structure analysis and stability evaluation are described in Section 4.

In the second part of the program, the requirement for development of a device with a high frequency performance greater than attainable with established devices such as the MODFET and heterostructure bipolar transistor (HBT) was addressed. The Bipolar Inversion Channel Field Effect Transistor (BICFET) is a proposed device which is conceptually capable of meeting those high frequency requirements and was the subject of investigations. Structurally, the BICFET has the same configuration as the HBT except that it has no physical base region. In the BICFET, an effective ultra-thin base (source) is formed by an electrostatically induced inversion layer. In order to produce the band structure favorable for creating an inversion layer, a highly doped spike layer is inserted in between the collector and wider band gap emitter layers. Since the induced inversion layer is very thin (~ 100Å), the charge transit time through this region is very small and therefore the device has the potential to operate at very high speed. Moreover, since the BICFET does not have a base, it should not suffer from the charging time delays of large base-emitter diffusion capacitances found in conventional HBTs. A further advantage of the BICFET is that the device should be able to exhibit transistor characteristics as soon as an input signal is applied and should not be limited by the signal propagation time delay associated with the full length of the source channel.

As in the case of the MODFET, the $Al_xGa_{1-x}As/GaAs$ material system can also be used for BICFET fabrication. For x-values less than ≤ 0.6 the material combination is favorable for n-channel device fabrication whereas, for high x-values, p-channel device structures can be made. Other material combinations can also be used providing that there is a significant difference between the conduction band and valence band edge discontinuities. This requirement arises from an analytical formulation which predicts the gain to be proportional to the exponential value of the band gap discontinuity difference.

In this program, a theoretical stuoy was undertaken to simulate device performance and provide a guide for optimum material and device structure parameters. Both semi-analytical and finite difference numerical simulations were carried out in one-dimension. DC device characteristics and space-charge distributions were extracted from the simulations. A preliminary BICFET test pattern mask set was designed and fabricated and process development using MBE material structures was carried out. The results of the theoretical work and process development work are described in Section V.

SECTION II
MODFET FABRICATION AND CHARACTERIZATION

2.1 MODFET MASK SET

At the commencement of the program, a mask set was designed which could be used for fabrication of MODFETs and associated processing and material test structures. These structures included elements for evaluating "backgating" and a few simple circuits for switching speed evaluation. The mask layout consisted of an array of 2.3 by 2.3 mm^2 dies, each of which had test structures and circuits laid out within an array of 16 by 16 probe pads. The probe pads (75 by 75 μm^2) were spaced at 125 μm intervals so that automated measurements using a 4 by 2 probe card could be carried out. The levels of the mask set are listed below:

1. Mesa A (All patterns)
2. Mesa B (All patterns except isolation and backgating)
3. Gate
4. Source/Drain Implant
5. Load Implant
6. Source/Drain Metallization
7. Contact Metallization
8. Via
9. 2nd Level Metallization

Levels 1 and 2 could also be used for ion-implantation isolation which formed an integral part of the MODFET isolation investigations. For fabrication of discrete devices and test structures, which were of principal interest in the program, only levels 1 to 7 were required. Levels 8 and 9 were used for ring oscillator and divide by two circuit fabrication. The composite die layout of the MODFET mask set is shown in Figure 2.1. Expanded plots of the various structures in the die are shown in Figures 2.2 through 2.6. Figure 2.2 shows the gated and ungated six point Hall Bar and Van der Pauw patterns. These were used for characterization of the electrical properties of heterostructure material both in terms of sheet values and as a function of depth. Figure 2.3

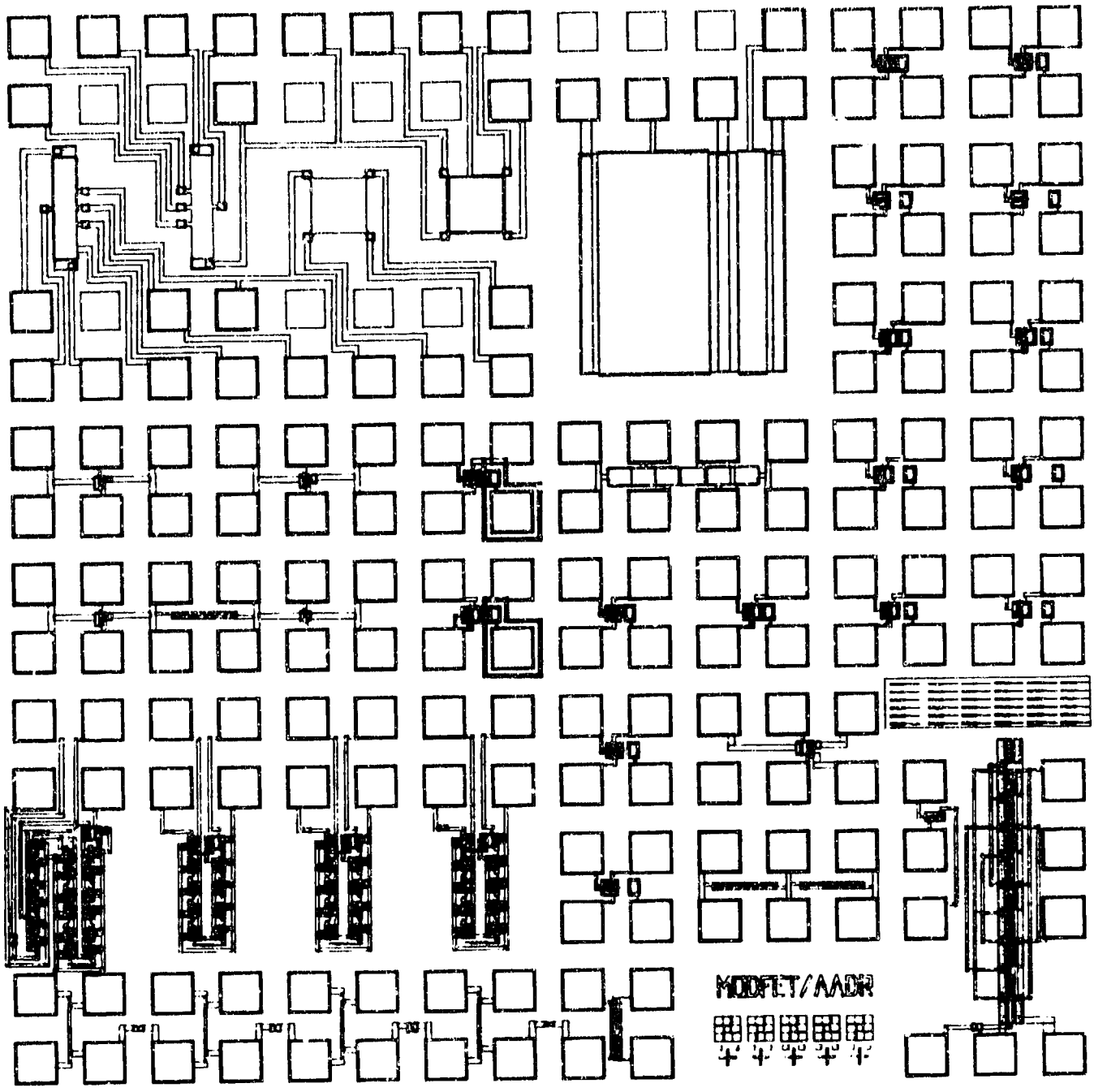


Figure 2.1 Composite die layout of MODFET mask set.

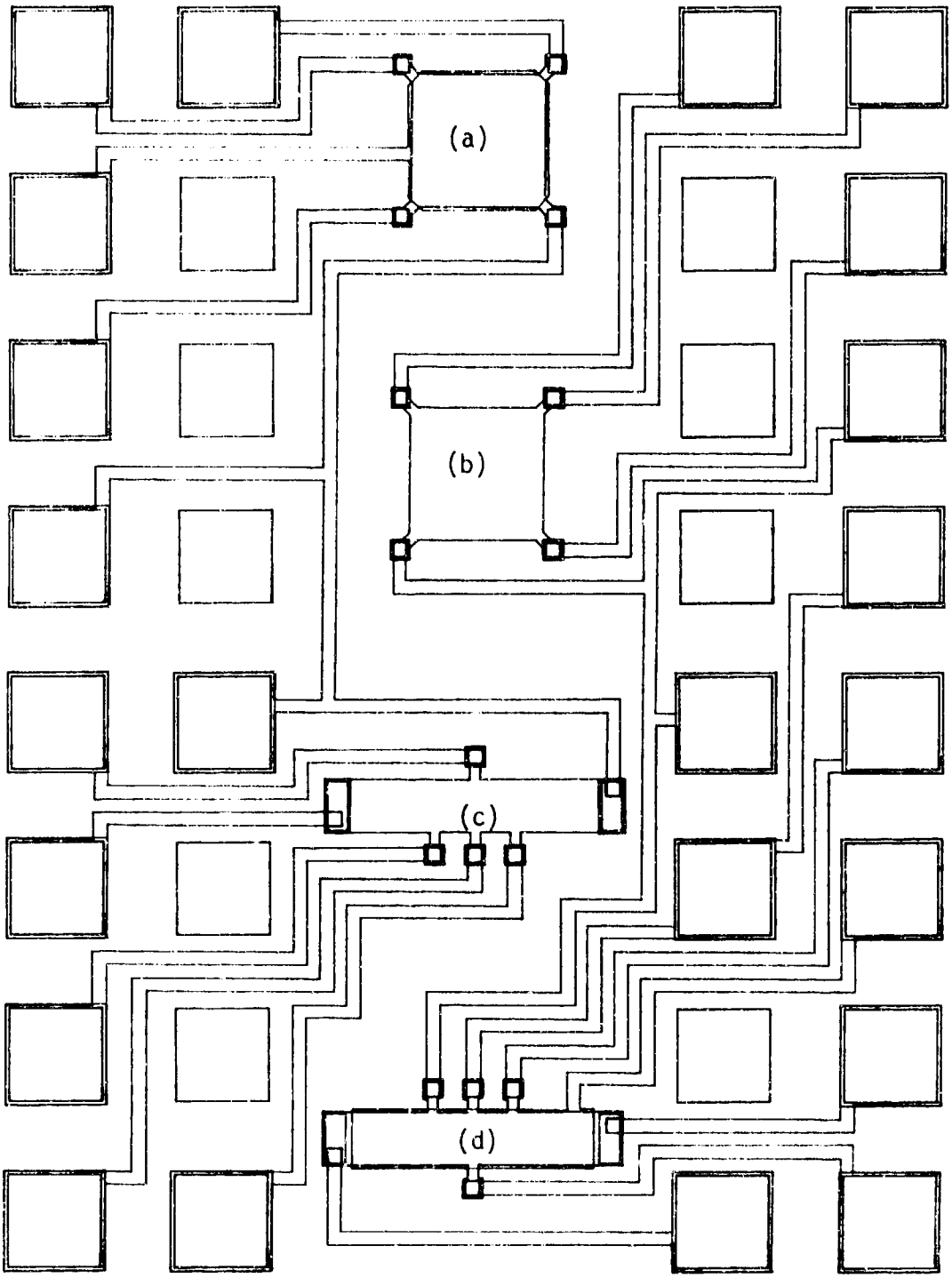


Figure 2.2 Layout of (a) gated Van der Pauw (b) Van der Pauw, (c) Hall bar, and (d) gated Hall bar patterns.

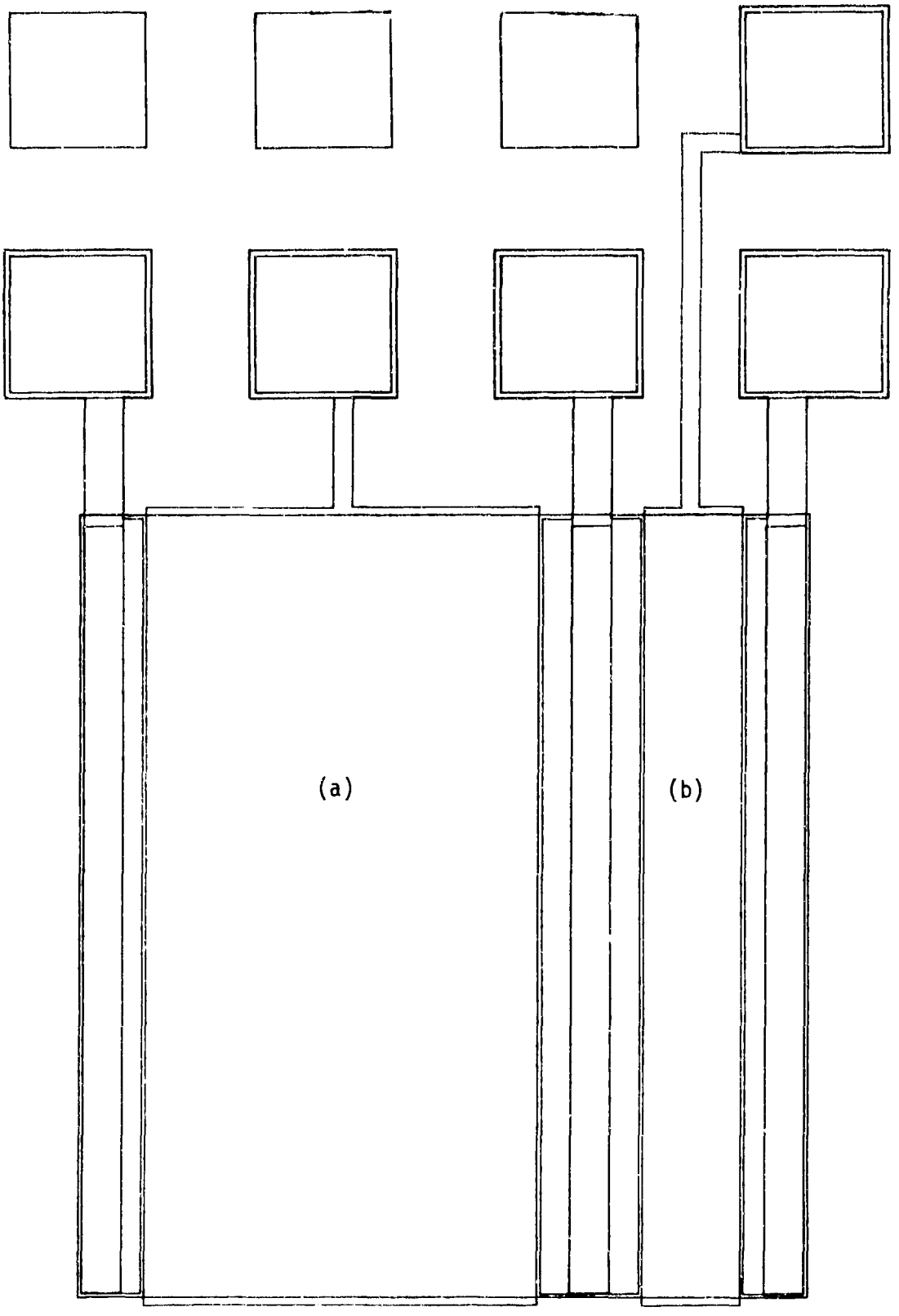


Figure 2.3 Fat FET structures with (a) 200 μm x 400 μm and (b) 50 μm x 400 μm gate areas.

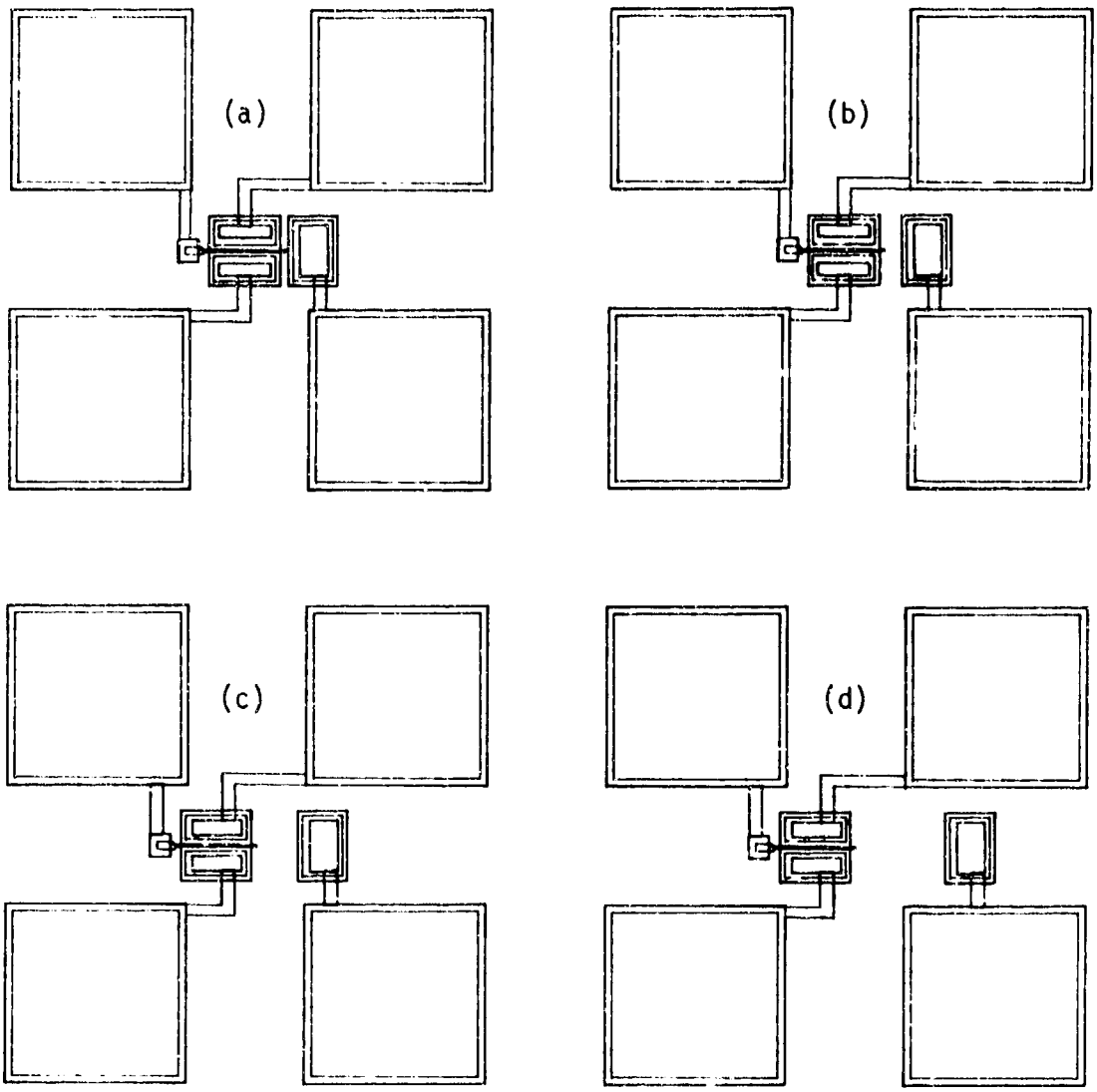


Figure 2.4 MODFET structures with endgate spacings (a) 2 μm, (b) 10 μm, (c) 20 μm, and (d) 40 μm.

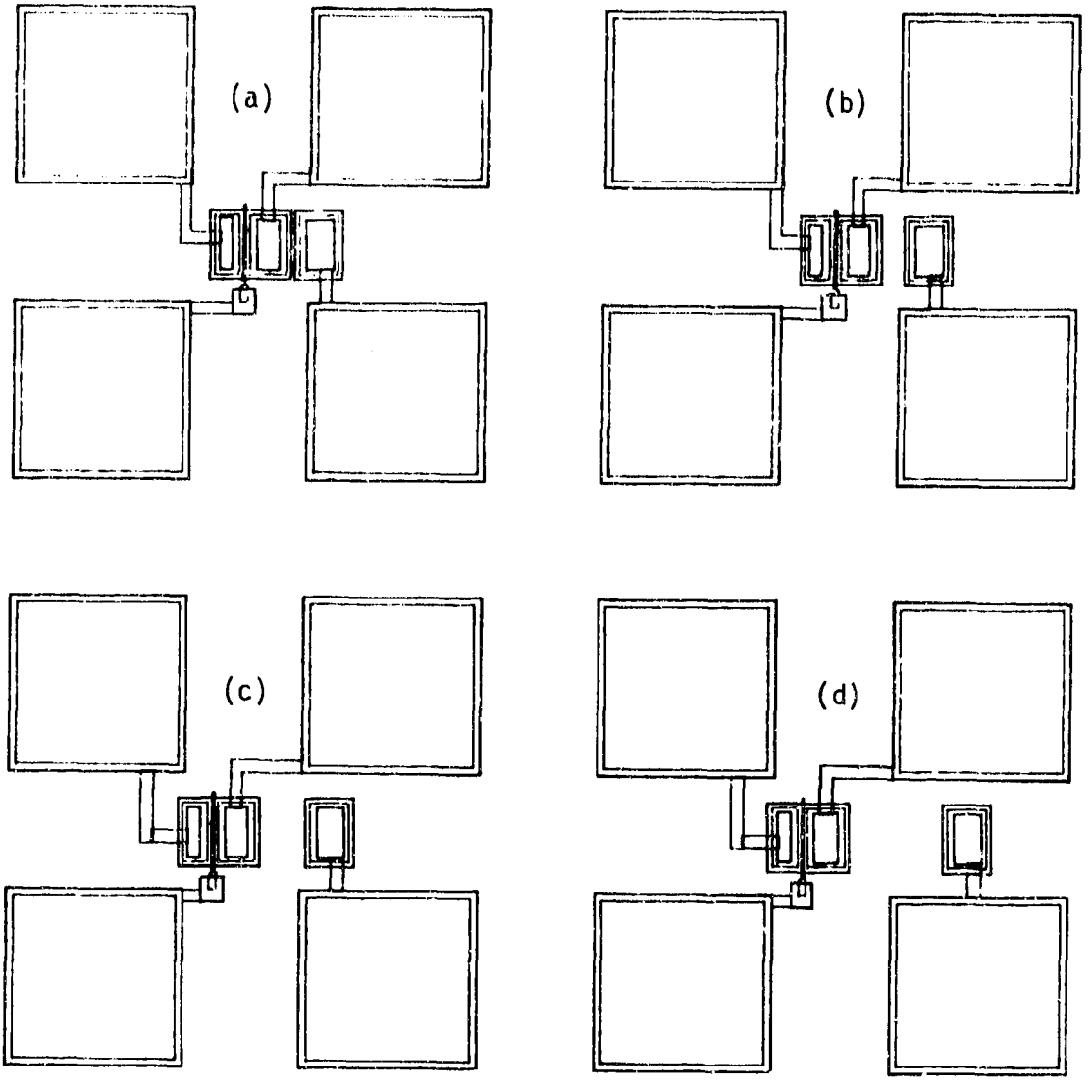


Figure 2.5 MODFET structures with sidgate spacings (a) 2 μm, (b) 10 μm, (c) 20 μm, and (d) 40 μm.

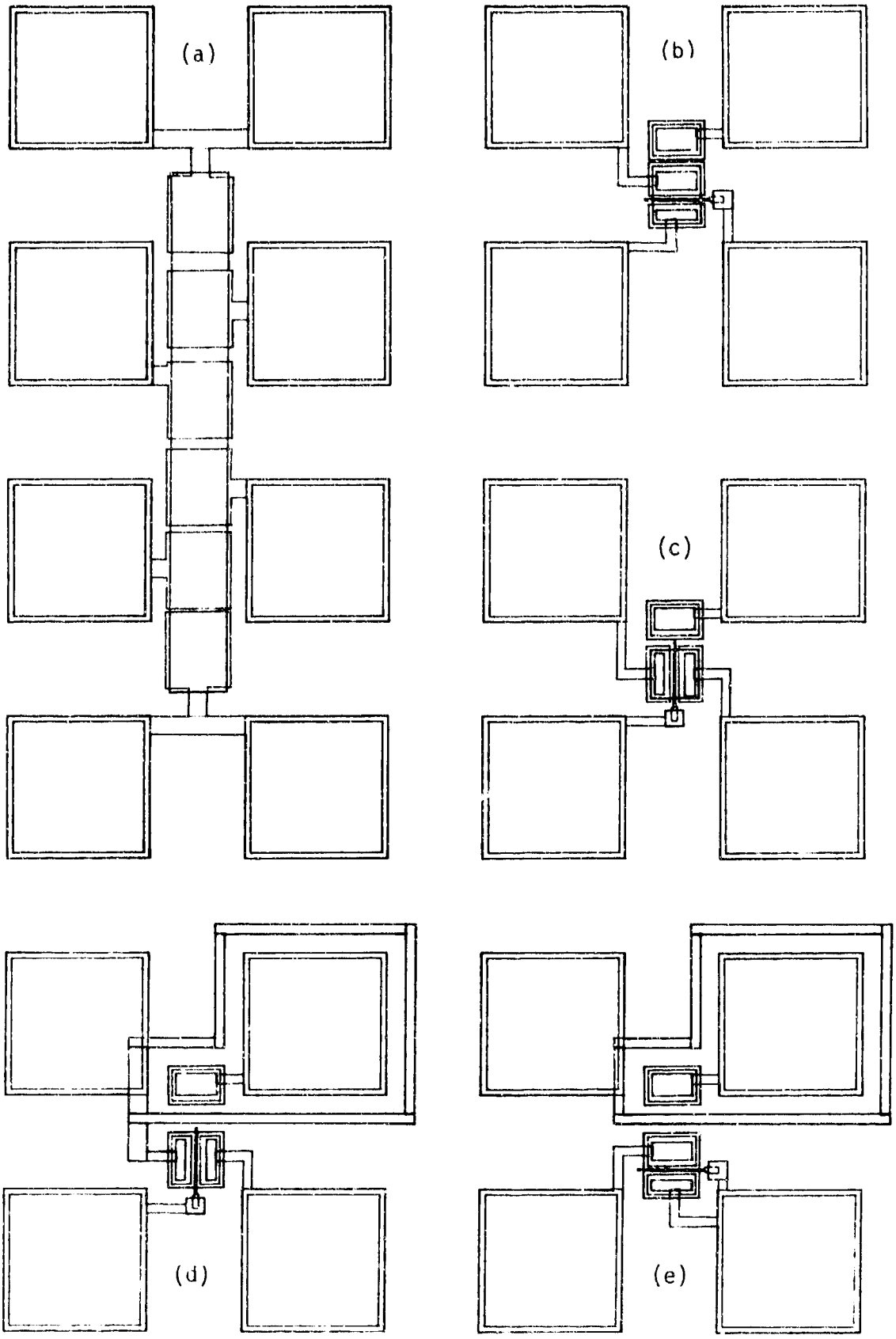


Figure 2.6 Layouts of: (a) contact resistance measurement (TLM) pattern, (b) and (c) type II MODFETs with 2 μm backgate spacings, (d) and (e) type I MODFETS with guard rings around backgate.

shows fat FET structures which had gate areas of 50 by 400 μm^2 and 200 by 400 μm^2. The patterns were used for large gate MODFET I-V and C-V characterization. For evaluation of the backgating effect in MODFETs, a series of structures was included having two basic MODFET structures and MODFET-backgate spacings ranging from 2 to 40 μm. Figure 2.4 shows the series for type I MODFETs in which the ohmic metallization lay within the isolation boundary leaving a 2 μm unisolated border. In this series the backgate, referred to as "end-gate," was located at varying distances from the end of the FET. An alternative series of structures, where the backgate, referred to as "side-gate," is located to the side of type I MODFETs, is shown in Figure 2.5. Type II MODFETs, in which the source/drain metallization overlaps the isolation boundary by 2 μm, are shown in Figure 2.6. Here, both end-gates and sidegates are shown for 2 μm backgate-MODFET spacings. In addition, Figure 2.6 also shows two type I MODFETs where the backgate is isolated from the MODFET by a guard ring. All the MODFETs, apart from fat FETs, included in the mask set were based on 1 μm gate length and 5 μm source-drain spacing geometries. The Transmission Line Model (TLM) pattern used for measuring contact resistances is shown in Figure 2.6. The contact spacings were 2, 4, 6, 8, and 10 μm.

Other elements included in the MODFET mask set were

Inverters (variable implanted loads)
High speed MODFET (high frequency testing)
Dual gate MODFET
Dual gate Inverter
Ring oscillator (fan out 1, variable implanted loads)
Ring oscillator (fan out 2)
Divide by two circuit
Metallization resistivity bridge
Dielectric isolation pattern
Inverter load resistors
Inter-metal resistivity pattern

The chrome mask set was fabricated by Micro Mask, Inc. using e-beam lithography processing and was compatible with all contact lithography processing at AFWAL/AADR.

2.2 BASIC TEST STRUCTURE MASK SET

Initial process development and MODFET fabrication were carried out using a basic test structure mask set which was available at the beginning of the program. Although the mask set was originally designed for GaAs MESFET processing due to the similarity between MESFET and MODFET processing technologies, the mask set was utilized without any major modifications. A schematic outline of the mask set is shown in Figure 2.7. The basic elements included in the test pattern are

A ... Fat FET - gate length 50 μm, width 400 μm
B ... Contact resistivity pattern - 2,3,4,5,6,8,10 μm pad spacings
C ... FETs - gate lengths 2,4,6,10 μm, width 100 μm
D ... Gated Van der Pauw pattern
E ... Van der Pauw pattern
F ... Gated Hall bar pattern
G ... Hall bar pattern

In this program, structure A was used for long gate MODFET characterization which included both current-voltage and capacitance-voltage measurements. Structure B was used for MODFET ohmic contact evaluation and structure C was used for DC characterization of MODFETs.

2.3 MODFET FABRICATION

2.3.1 Conventional Processing

The cross-sectional structure of a AlGaAs/GaAs MODFET fabricated by a "conventional" MESFET-type process is shown schematically in Figure 2.8. The corresponding band diagram under the gate is shown in Figure 2.9 for the case of (1) low gate reverse bias and (2) gate reverse bias equal to the threshold voltage. The ohmic contact metallization consisted of the sequential deposition of 50 Å Ni, 170 Å Ge, 330 Å Au, 150 Å Ni, 2000 Å Au by e-beam evaporation. In general, contacts formed directly to the n^+ $Al_xGa_{1-x}As$ of the MODFET structure were found to have nonuniform and excessively high contact resistances, even after prolonged alloying cycles. Consequently,

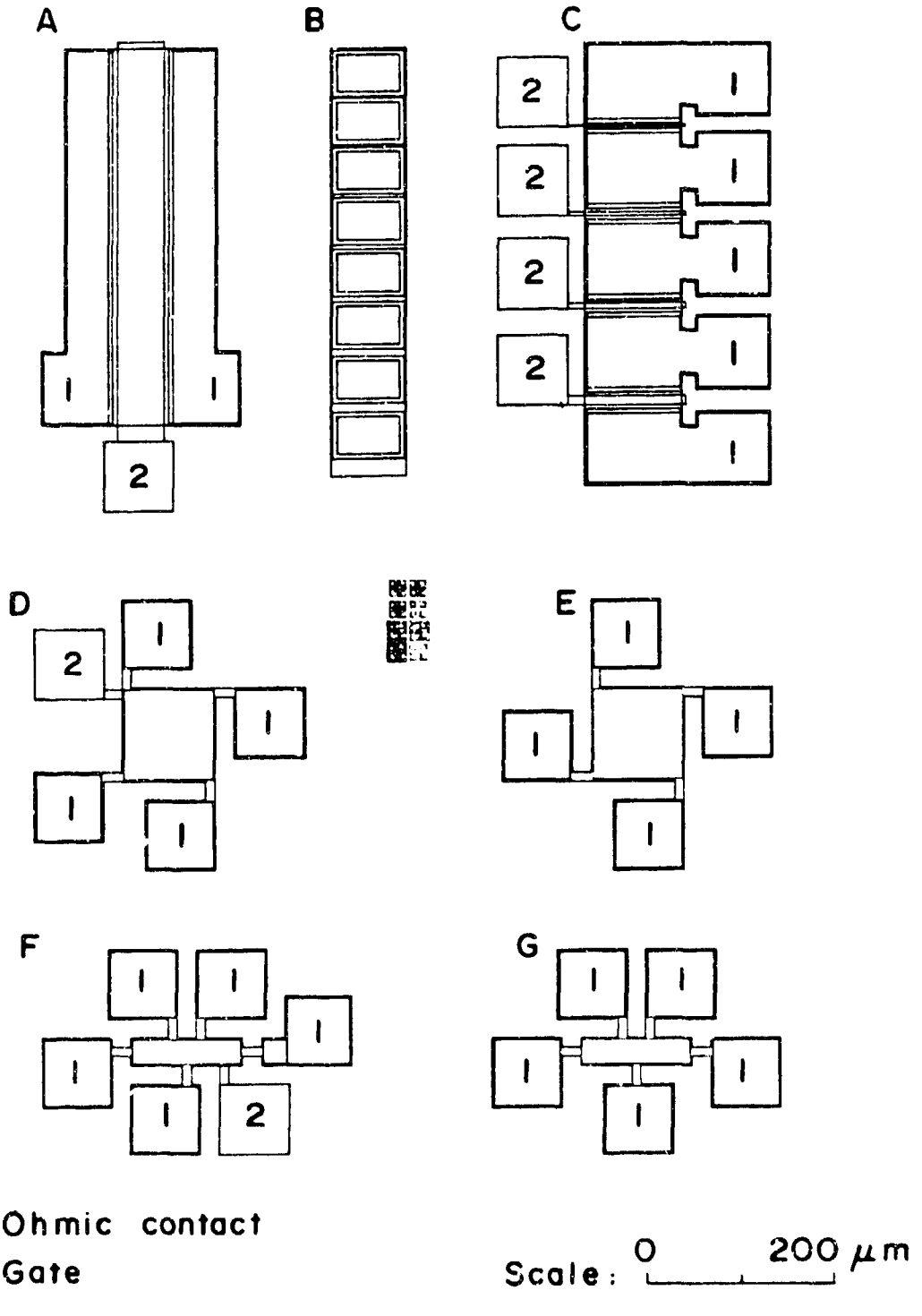


Figure 2.7 Die layout of basic test pattern mask set.

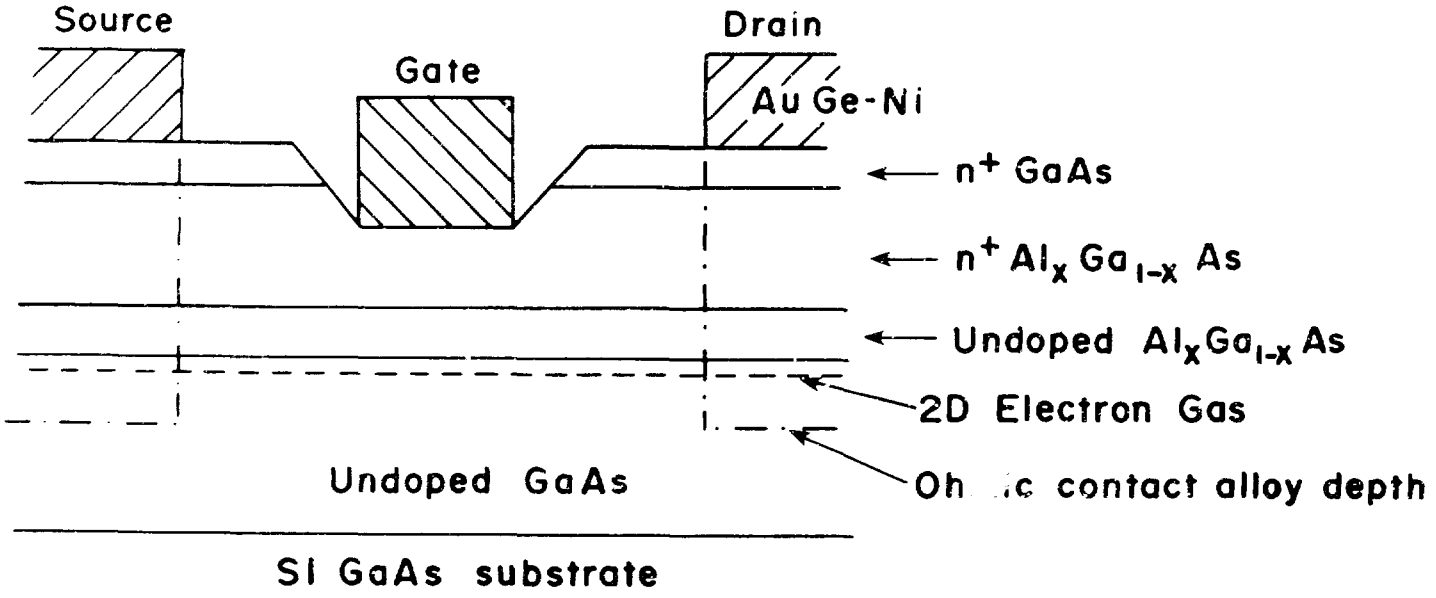


Figure 2.8 The cross section of a conventional MODFET structure.

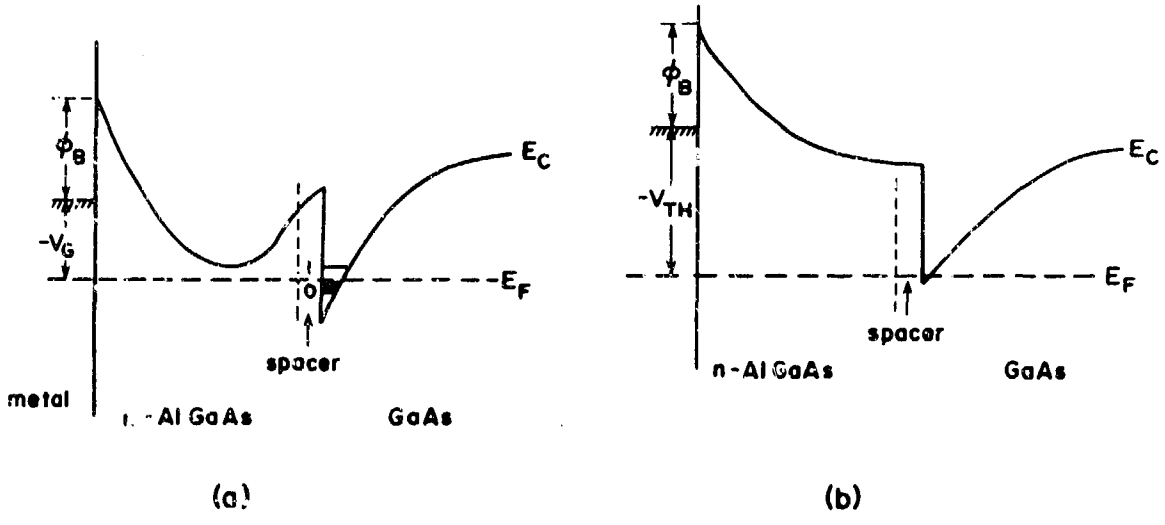


Figure 2.9 Band diagrams of modulation doped GaAs/AlGaAs heterostructure under (a) low reverse bias, (b) reverse bias $V_G = V_{TH}$.

a preliminary study was undertaken to determine what thickness of n^+ GaAs cap layer was required to minimize contact resistance. The MBE material used for this purpose had the following structure:

t Å	GaAs	($n = 1.6 \times 10^{18}$ cm^{-3})
380 Å	$Al_{0.3}Ga_{0.9}As$	($n = 1.6 \times 10^{18}$ cm^{-3})
25 Å	$Al_{0.3}Ga_{0.7}As$	(undoped)
0.9μm	GaAs	(undoped)

Semi-insulating GaAs substrate

Material with cap layer thicknesses, t, ranging from 0 to 410 Å was investigated. A conventional quartz tube furnace with flowing N_2 was used for the anneal. The anneal cycle consisted of a ramp time of ~ 2-1/2 minutes to the peak anneal temperature, a dwell time of 30 seconds and a subsequent cooldown in the cold zone of the furnace. The temperature of the wafer was monitored using a thermocouple in contact with a dummy GaAs sample located in close proximity to the metallized wafer. The peak anneal temperature ranged between 420 and 450°C, the former being an optimum for minimum contact resistance to n- GaAs. The contact resistance was measured using the TLM pattern and is plotted as a function of GaAs cap layer thickness in Figure 2.10. For t = 410 Å, the minimum contact resistance measured was 0.19 Ωmm whereas for t = 0 the contact resistance increased to ~ (2.5 - 3.1) Ωmm. The n^+ GaAs cap layer is believed to serve two purposes. First, it provides a material to which low resistance ohmic contacts can be formed reproducibly and, second, it eliminates the problems associated with fabricating ohmic contacts directly to AlGaAs. The difficulty in forming low resistance contacts to AlGaAs is not fully understood, although it may be partly attributed to an alloy impeding interfacial oxide. In the case of contact resistances measured to capped MODFET material, the resistance consists of a parallel combination of contacts to the n^+ GaAs cap layer, the n^- AlGaAs layer and the two-dimensional electron gas (2DEG). In the case of the 2DEG, contact may not be made directly and may involve current transport through the intermediate AlGaAs layer. From the results of this study, it was concluded that an n^+ GaAs cap layer of thickness $t \geq 400$ Å was necessary to ensure

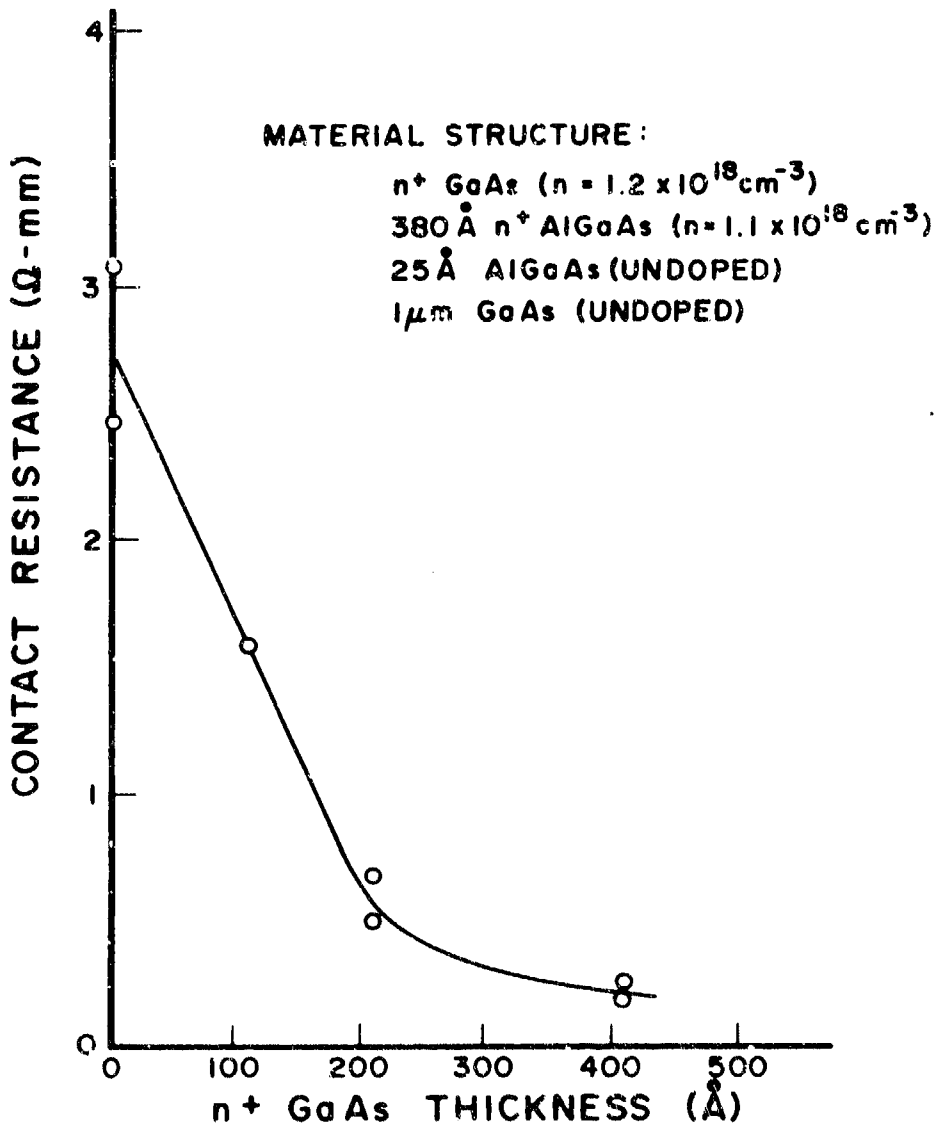


Figure 2.10 Variation of contact resistance of MODFET Ohmic contact with n^+ GaAs cap layer thickness.

low resistance ohmic contacts suitable for MODFET fabrication. Consequently, for all subsequently processed conventional MODFETs, material was used with t ≈ 400 Å.

The incorporation of an n^+ GaAs cap layer and the requirement for producing either enhancement or depletion mode MODFETs necessitate the use of a controllable and reproducible gate recess technique. The use of a selective recess etch would allow the mode of operation to be determined by the AlGaAs doping and thickness. For this purpose, an etchant consisting of 30 percent hydrogen peroxide buffered to a pH of 7.0 using 58 percent ammonium hydroxide solution was investigated. Etching was determined to be diffusion-rate limited which resulted in a faster etch rate of small area features compared with large area features (≈ 10 Å/sec). In addition, for a large area opening in a photoresist mask, the etch rate was enhanced near the edge of the mask. In the case of the MODFET structure, this variability in etching was evened out at the AlGaAs layer where the etch rate was considerably reduced. However, the etch stop process was not found to be instantaneous and appeared to be determined by the slower dissolution rate of the AlGaAs oxide surface boundary layer compared with that of GaAs. Dissolution in dilute HCl indicated that the AlGaAs oxide layer formed during the "over-etch" process could have a thickness up to ~ 250 Å. The formation of this oxide consumed a considerable fraction of the AlGaAs layer which meant that the mode of operation was no longer determined by the original AlGaAs parameters. In order to avoid the formation of a significant AlGaAs oxide layer, the etch rate and recess time had to be carefully controlled thereby losing the advantages of selectivity. In view of the problems associated with etch rate variability and the inability of the etch to stop precisely at the GaAs/AlGaAs interface, subsequent processing of MODFETs used a non-selective etch.

Gate recessing requires a controllable etch which produces a flat bottomed profile and does not attack photoresist to any significant degree. These requirements are met by the solution $3NH_4OH:1H_2O_2:1000\ H_2O$, which was used in all subsequent MODFET processing work. Since this solution does not have any appreciable etch selectivity of

GaAs over AlGaAs, the MODFET source-drain resistance and saturation current had to be monitored to determine the desired mode of transistor operation. The average recess etch rate was determined to be 6.5 Å/sec for a freshly mixed solution. For typical MODFET material with a 400 Å $Al_{0.3}Ga_{0.7}As$ layer ($n = 1.5 \times 10^{18}$ cm^{-3}) and a 25 Å $Al_{0.3}Ga_{0.7}As$ spacer layer, a saturation current of ~ 5mA per 100 μm gate width produced an E-mode device. In all of the MODFET fabrication work, the gate metallization consisted of 200 Å Cr:700 Å Pd:2,100 Å Au.

2.3.2 Self-Aligned Gate Processing

The self-aligned gate MODFET structure has a number of advantages over the conventional structure which was described in Section 2.3.1. As in the case of MESFET technology, the self-aligned gate approach has the potential to produce more uniform threshold voltages over the wafer area and also greater values of transconductance. The superior uniformity aspect arises from the fact that in the self-aligned gate process no gate recessing is required and consequently, the material structures establishes the threshold voltage of the transistor. Since the semiconductor layer thicknesses and doping concentrations can be controlled to better than 5 percent by advanced MBE and MOCVD growth techniques, the degree of threshold voltage uniformity should also be of the same order. The transconductance can also be enhanced compared with the conventional structure by reducing the source series resistance by ion implantation doping. This process effectively reduces the dependence of device performance on gate/source-drain alignment. In addition, the self-aligned gate process can be used to tailor the gate length to submicron dimensions which also enhances the transconductance. The advantages afforded by a greater degree of device uniformity and transconductance translate into higher performance high frequency circuits.

The basic cross section structure of a SAG-MODFET is shown schematically in Figure 2.11. The initial starting material used in these investigations was grown by molecular beam epitaxy and had the following structure:

330Å	$Al_{0.3}Ga_{0.7}As$	($n = 1.5 \times 10^{18}$ cm^{-3})
76Å	$Al_{0.3}Ga_{0.7}As$	(undoped)
1μm	GaAs	(undoped)
S.I. GaAs		

This structure was chosen in order to obtain enhancement mode MODFETs. The basic processing steps adopted are listed as follows:

1. Mesa isolation
2. Refractory gate metal deposition
3. Plasma etch gate delineation
4. Source/drain ion implantation
5. Rapid thermal anneal
6. Source/drain metallization
7. Ohmic contact anneal
8. Interconnect/probe pad metallization

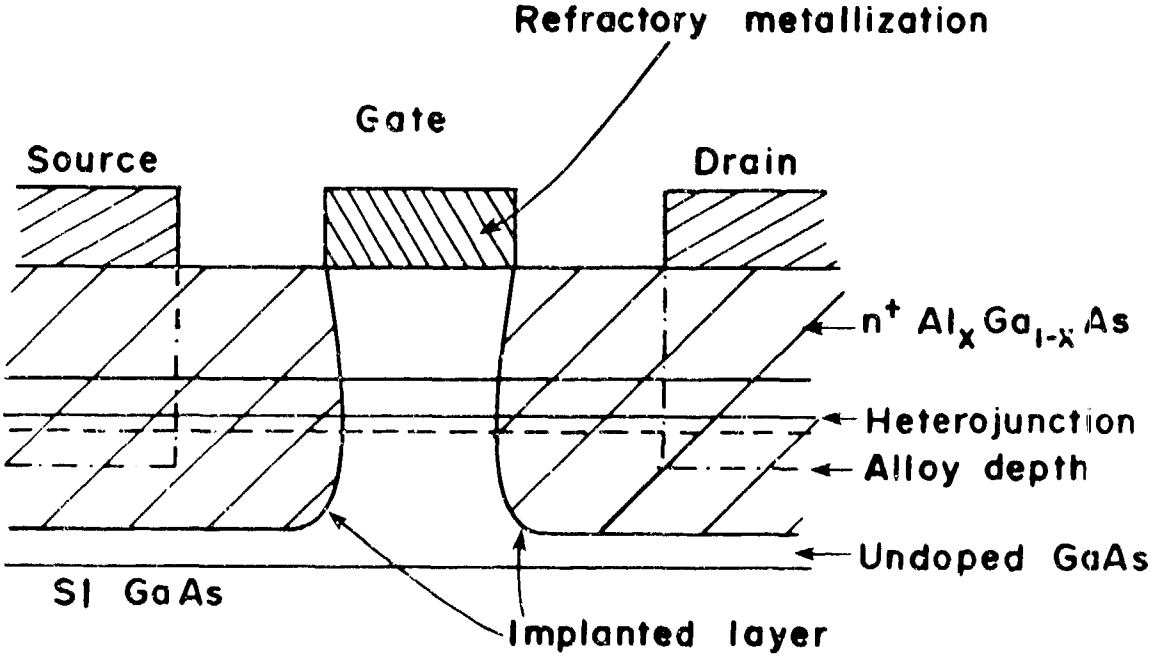


Figure 2.11 Cross section of a self-aligned gate MODFET structure.

The steps 1, 6, 7, and 8 were the same as used in the conventional MODFET processing scheme. The other processing steps will be discussed in the following sections.

2.3.3 Refractory Metal Gate

Since the starting material contains no cap layer, the 2DEG interface is located closer to the surface of the material compared with the conventional MODFET structure. This, in turn, makes the active device area more susceptible to process induced damage and, therefore, care needs to be taken in order to minimize damage and thereby preserve the uniformity and electrical characteristics of the epitaxial material. The choice of the refractory metal gate and the deposition process are important parameters for the SAG-MODFET. WSi_x was chosen as the refractory metal since for $x \simeq 0.64$ it was reported to be relatively stable on GaAs, both in terms of barrier height and interface integrity, at temperatures up to 850°C [1]. The reported barrier height and ideality factor for as-deposited contacts on GaAs ($n = 2 \times 10^{17}$ cm^{-3}) were $\simeq$ 0.75 eV and $\simeq$ 1.1, respectively. The value of $x = 0.64$ was found to be the optimum for producing the best stress-free mechanically matched films on GaAs. This was demonstrated by adhesion tests at high temperatures which were found to fail at $x = 0.4$ and $x = 0.8$ due to excessive compressive and tensile stress, respectively. Although similar tests have not been reported on AlGaAs, the fabrication of SAG-MODFETs with good electrical performance has been demonstrated [2].

In this program, the sputtering system used for refractory gate metal deposition was a Perkin Elmer Model 2400-6J. The option of co-sputtering was not available in this system. In order to select the best target for the SAG process, W_xSi_y films were sputter deposited on Si substrates (in an argon plasma) from a number of available W/Si targets. In particular, targets with rated compositions of $W_{62.5}Si_{37.5}$, $W_{55.6}Si_{44.4}$ and WSi were tested. The RBS spectrum of the film deposited using the 50/50 W/Si target is shown in Figure 2.12. The composition of the film deduced from RBS analysis was $WSi_{0.74}$. One percent oxygen was also found as a contaminant from the sputtering

process. The 50/50 W/Si target was used for all subsequent processing. Initial experiments indicated that the sputter deposited W_xSi_y films suffered from adhesion problems on GaAs substrate. A brief sputter etch prior to the sputter deposition was sufficient to promote adhesion of W_xSi_y to GaAs substrates. Since the surface layer of the SAG/MODFET is a very thin (~330 Å) AlGaAs layer, the sputter etch rate was calibrated for AlGaAs. The sputter etch rate of MBE grown AlGaAs was 223+/-6 Å/min. compared to 159+/-25 Å/min. for GaAs at 50 watt RF power and 10 mTorr Ar pressure. Although adhesion of W_xSi_y on sputter etched AlGaAs samples was good, the same sputter etch step on the MODFET material produced extensive and irreversible radiation damage to the 2DEG as manifested by complete carrier compensation.

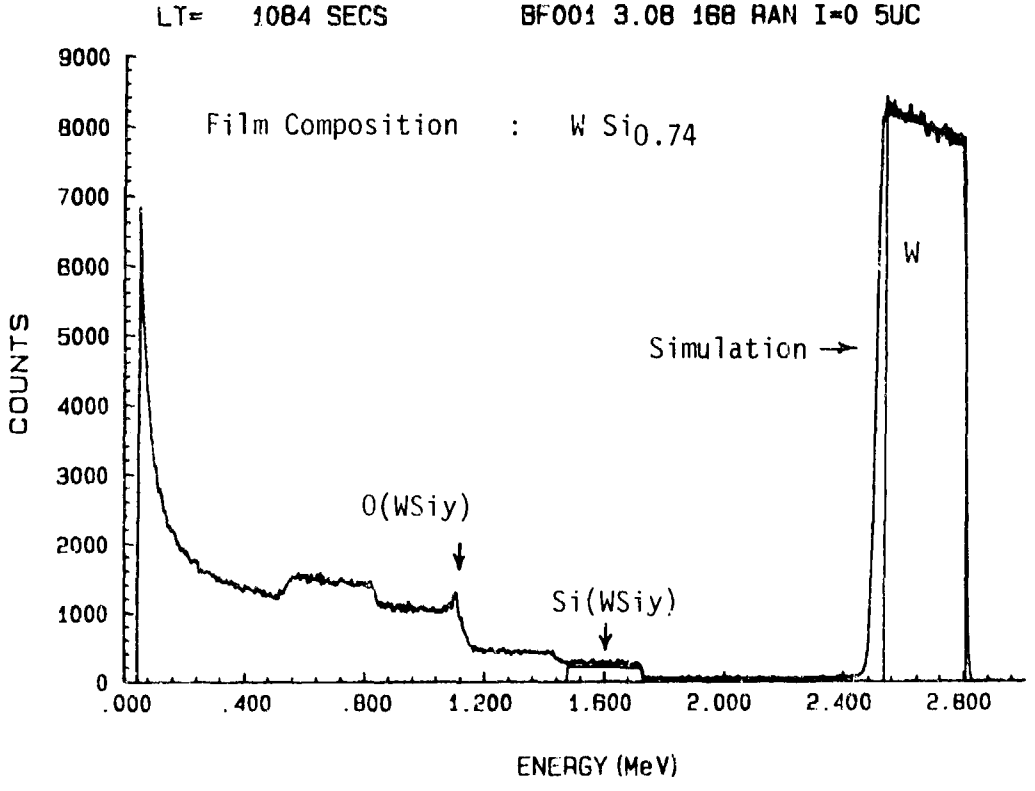


Figure 2.12 RBS spectrum obtained from $W_{50}Si_{50}$ target sputter deposited film (200 W, 10 mTorr)

In the absence of a magnetron sputtering system, which could minimize radiation damage to the substrate, the sputter etch step was eliminated from the SAG-MODFET process. This intensified the silicide adhesion problem and lead to a complete review of the SAG process. In particular, the self-aligned gate had to fulfill the following requirements:

1. Schottky diode behavior
2. Good adhesion
3. Mask against ion implantation
4. Withstand annealing cycles.

Since good adhesion is a direct function of surface treatment, a number of GaAs samples were therefore processed under different chemical surface treatment conditions. W_xSi_y was then sputter-deposited and the scotch tape test (STT) was used to evaluate adhesion. These experiments indicated that a 15 second $1HCl:1H_2O$ etch followed by a 30 second DI water rinse and air exposure limited to 2 minutes before loading the samples into the sputtering system ensured good adhesion of the deposited films.

A second requirement is a low resistivity silicide film which is a function of the film composition which depends strongly on the film deposition conditions. To evaluate the optimum sputter deposition conditions, the RF power as well as the pressure of the Ar gas were varied. Care was taken to ensure that the base pressure in the sputtering system was always in the 10^{-7} torr range. The deposited films were subjected to a sheet resistance measurement by a four-point probe and the STT both before and after the RTA cycle.

In a first set of experiments, the RF power was held constant at 500 watts and the Ar pressure was varied from 5 to 20 mTorr. The deposition rate is shown in Figure 2.13. Shown in Figure 2.14 are the measured resistivities of the films before and after RTA at 800°C for 20 seconds. Although the resistivity of all the films was high as deposited, there was a considerable reduction after RTA. The adhesion of

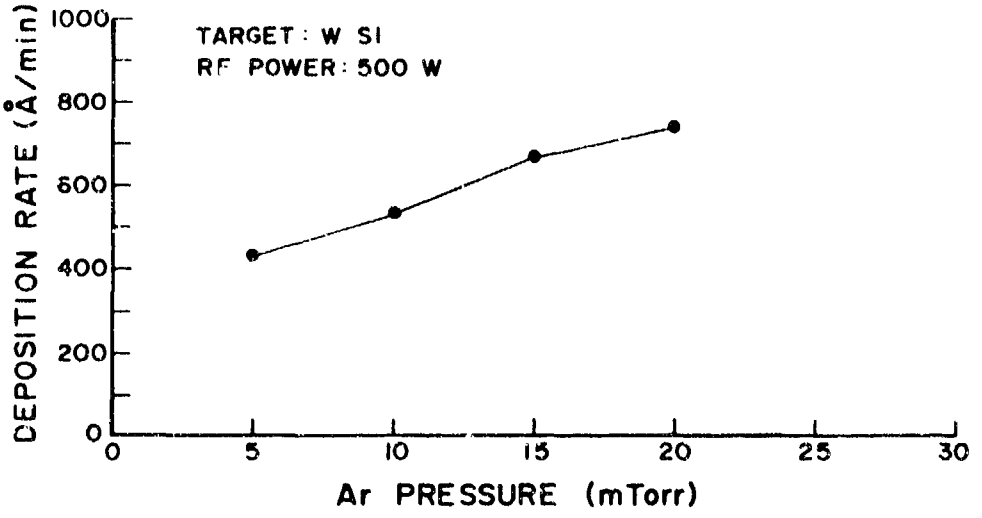


Figure 2.13 Deposition rate of W_xSi_y films vs Ar pressure at 500 W RF power.

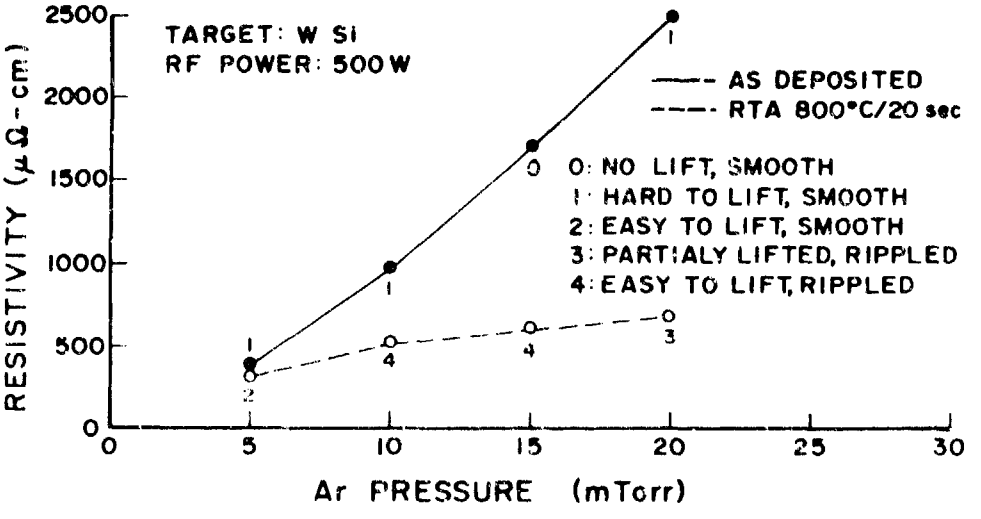


Figure 2.14 Resistivity and adhesion of W_xSi_y films deposited at 500 W RF power vs Ar pressure.

the films as determined by the STT, is rated and a number is displayed next to the data points according to the table shown in the insert of Figure 2.14. With the exception of the 5 mTorr run, all the films have acceptable adhesion as deposited but failed the STT after RTA. In most of the samples that failed the STT test, the silicide film rippled and/or bubbled. The ripples are typical of compressive stress of W_xSi_y films on GaAs. This result indicates that the mechanical properties of the refractory film are not only dependent on the composition, but also on the particular sputtering system and deposition parameter employed.

The effects of RF deposition power on the measured resistivity of the W_xSi_y films are shown in Figures 2.15 and 2.16. The Ar pressure in Figures 2.15 and 2.16 was 10 and 5 mTorr, respectively. Figure 2.17 shows the deposition rate for these cases, which as expected, increases as the RF power increases. The dotted lines in Figures 2.15 and 2.16 show the resistivities of the films after RTA at 800°C/20 sec. For the 10 mTorr pressure case, shown in Figure 2.15, the as-deposited films were excellent. After RTA, however, the films rippled and bubbled and failed the Scotch tape test. For the 5 mTorr case, after RTA, the films did not show any evidence of stress buildup, i.e., no bubbles or ripples appeared. In addition, for RF powers of 100 and 200 watts, adhesion was good after RTA. In conclusion, a 5 mTorr Ar pressure at either 100 or 200 watts appeared to fulfill the SAG requirements.

2.3.4 Plasma Etch

A plasma etch was used to delineate the W_xSi_y gates. The plasma etch system consisted of a planar reactor with a RF operating frequency of 30 KHz. The gas used was a mixture of CF_4 with 8 percent O_2. The best results were obtained at flow rates of 46 sccm and 4 sccm for CF_4 and O_2, respectively, at 200 mTorr pressure. The plasma power was 25 watts, which was the smallest possible for attaining a plasma in the available system. The reason for using this low power was to minimize the radiation damage to the sensitive 2DEG. The etch rate of the W_xSi_y film at this power setting was approximately 267 Å/min.

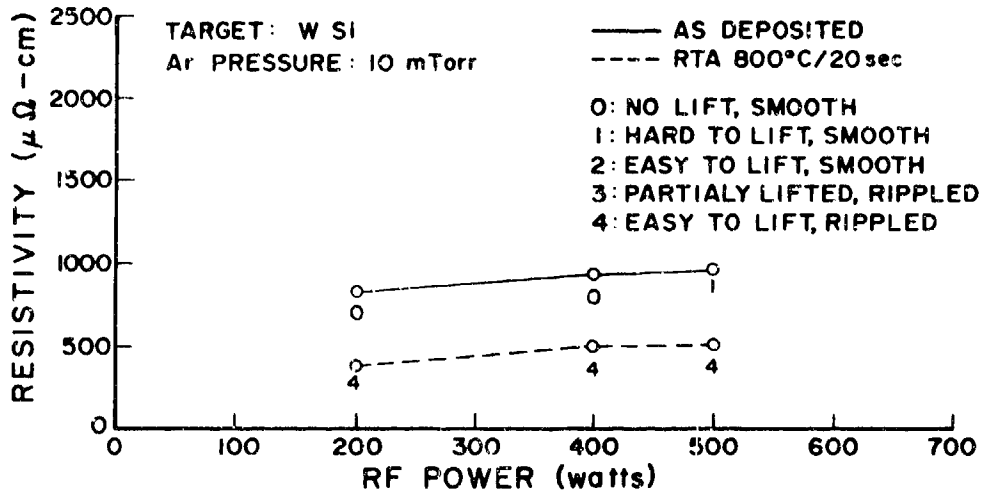


Figure 2.15 Resistivity and adhesion of W_xSi_y films deposited at 10 mTorr vs RF power

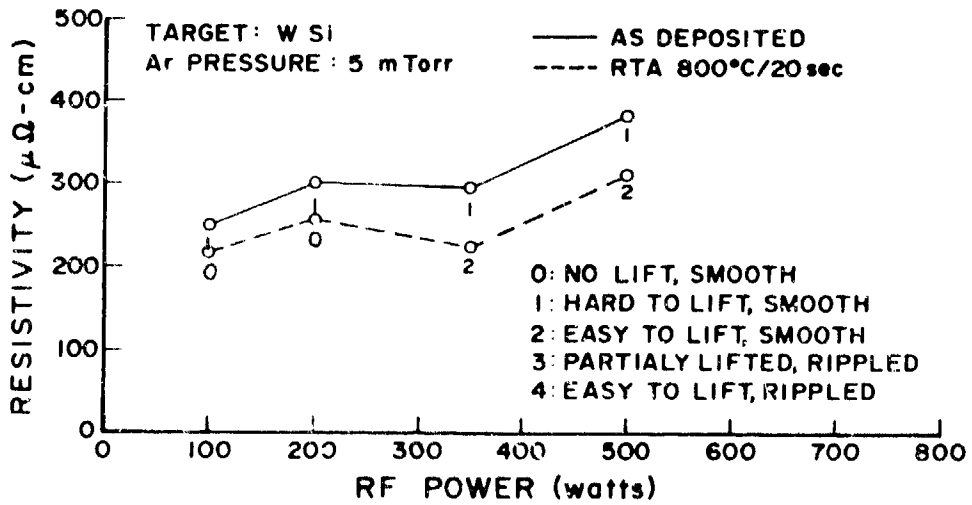


Figure 2.16 Resistivity and adhesion of W_xSi_y deposited at 5 mTorr vs RF power

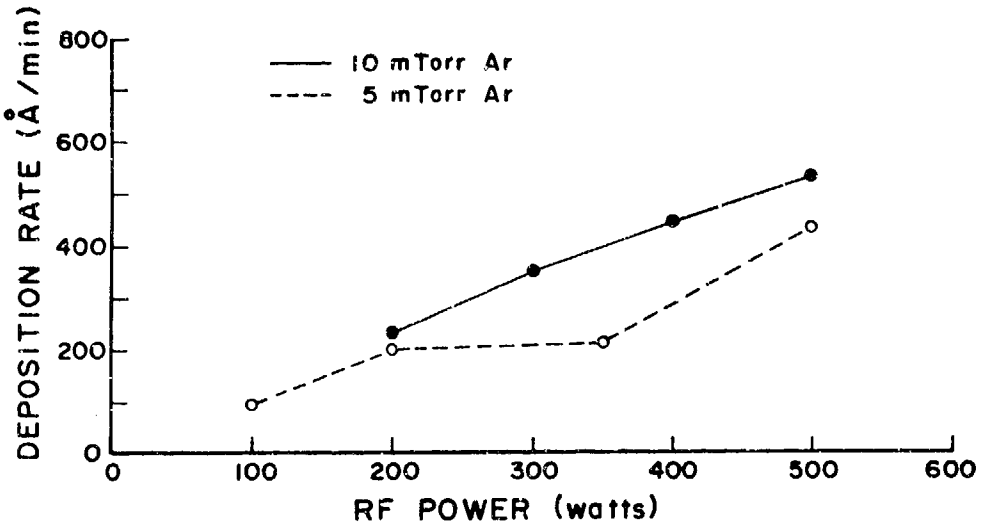


Figure 2.17 Sputter deposition rate of W_xSi_y at 5 and 10 mTorr Ar pressure

Using a photoresist gate mask, etched profiles were vertical with no visible undercut of the 1-μm length gate mask.

2.3.5 Ion Implantation

The purpose of the ion implantation step is to reduce the source- and drain-gate series resistances and to form a sufficiently highly doped layer to which low resistance ohmic contacts can be fabricated. Since the 330Å AlGaAs layer was already doped to 1×10^{18} cm^{-3}, further significant increases in the doping level and conductivity of this layer by ion implantation would be difficult to attain. However, by implanting donor atoms into the GaAs buffer layer to a depth of ~ 2,000 Å, a low resistance layer could be formed which would form direct contact with the 2DEG under the gate. From LSS range statistics, a silicon dose of 2×10^{13} cm^{-3} at energies of 100 or 200 keV would meet the requirements of doping in the source and drain regions such that the sheet resistance was ≤ 300 Ω/□. In these investigations, the thickness of the gate was 2000 Å which was believed to be sufficient for a W_5Si_3 mask against a 2×10^{13} cm^{-3} dose of 100 keV Si ions.

2.3.6 Implantation Anneal

After the ion implantation step, a thermal anneal cycle is required in order to anneal out the incurred radiation damage and activate the implanted species. Conventional furnace annealing at ~ 800°C for 15 m requires some form of surface passivation such as a dielectric cap or an arsenic vapor overpressure. Initial investigations on the use of Si_3N_4 cap layers formed by either pyrolytic chemical vapor deposition or plasma enhanced chemical vapor deposition were unsuccessful due to excessive stress in the films which caused lifting of the gates during annealing. In the absence of an arsenic overpressure anneal furnace, rapid thermal annealing using a Heatpulse 210 system was investigated as an alternative implant activation technique. This technique involved placing the metallized/implanted wafer face to face with a blank polished GaAs wafer on a silicon support wafer.

In order to optimize the Rapid Thermal Anneal (RTA) sequence for activating the implanted source and drain regions, undoped MBE GaAs samples were implanted at 200 KeV with a Si dose of 2×10^{13} cm^{-2} and subsequently annealed at 775, 800, 825, 850 C for 30 seconds and 850, 875, 900, 925°C for 5 seconds. The results from Hall measurements are shown in Figure 2.18. The variation of the Hall results with the different RTA cycles was small, indicating that all of the RTA cycles examined were suitable for the implant activation. In particular, the implant activation efficiency was ~ 75 percent, the sheet resistance was ~ 130 ohm/sq, with the exception of the 925°C, 5 second cycle which was 153 ohm/sq, and the mobility was ~ 3300 cm^2/V seconds. On the basis of these results and taking into account the requirement of minimal gate degradation, 800°C/20 second was selected as the optimum RTA cycle.

2.3.7 SAG MODFET Results

Figure 2.19 shows a picture of the I-V characteristics for a nominally 1 μm gate length prototype SAG-MODFET fabricated using a 2000 Å thick W_xSi_y gate. Figure 2.20 shows the I-V characteristics of the W_xSi_y gate, demonstrating Schottky behavior. The transconductance of this particular device was 127 ms/mm. From

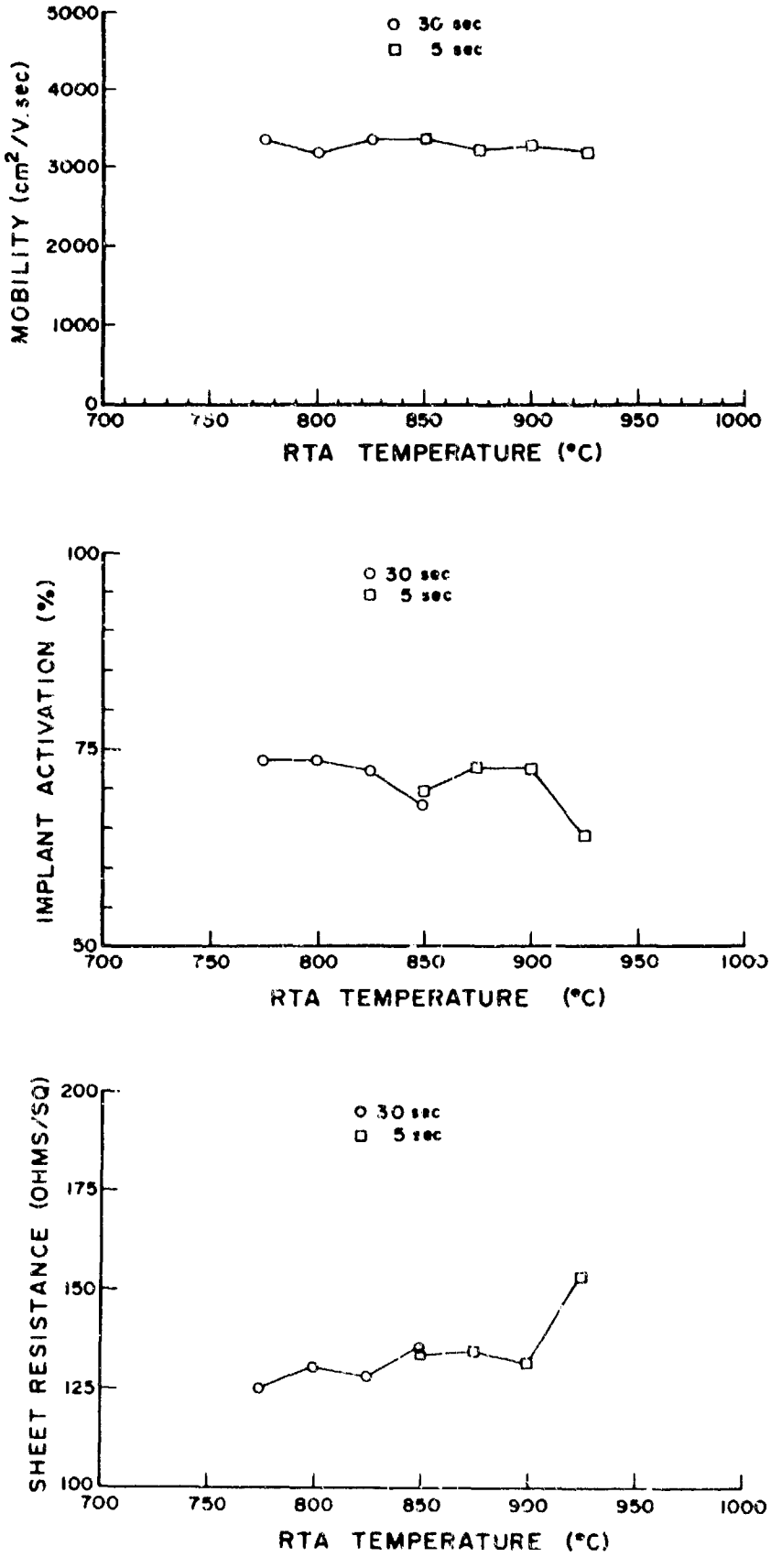


Figure 2.18 Hall measurement results on RTA ion implanted GaAs.

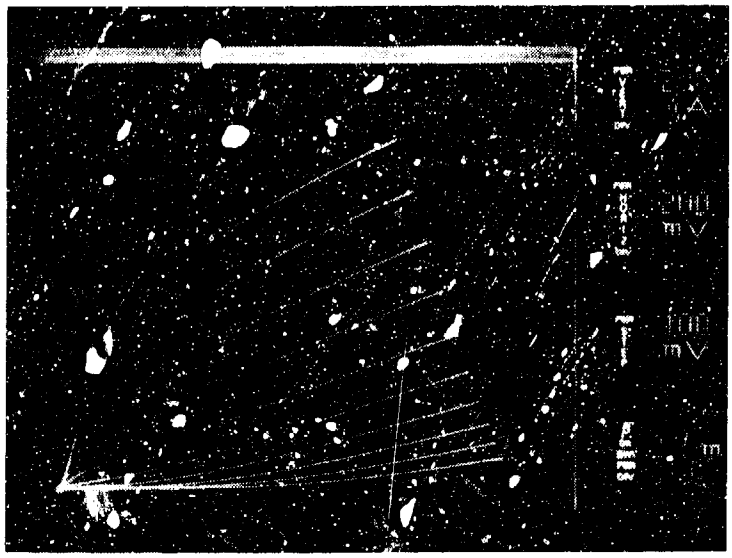


Figure 2.19 SAG-MODFET current-voltage characteristics.

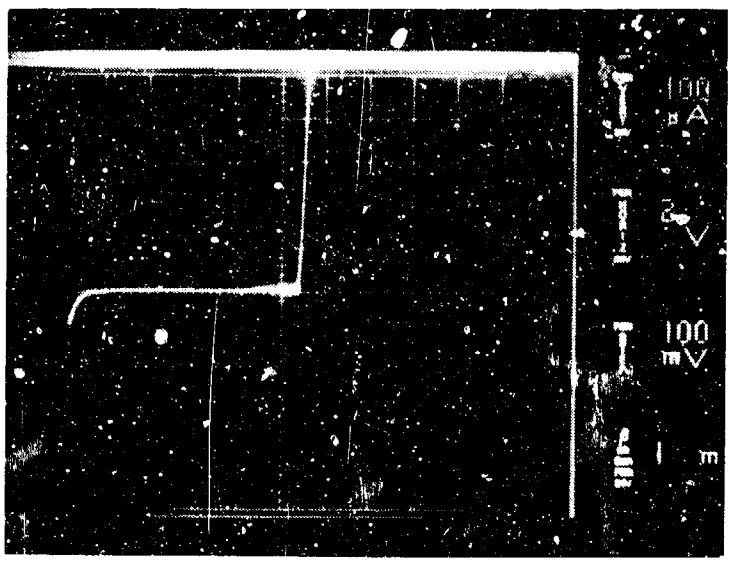


Figure 2.20 Current voltage characteristics of the SAG-MODFET gate.

Figure 2.19, it can be observed that the current does not saturate, and for low-gate biases, the current shows a threshold dependence on the drain voltage. From FET studies, this is typical of short channel effects and subthreshold behavior.

SECTION III
MODFET ISOLATION

3.1 BACKGATING IN MESA ISOLATED MODFETS

In ion implanted GaAs MESFETs, backgating is an important consideration in the design of GaAs integrated circuits [3]. The backgating effect is characterized by a threshold voltage, above which a large increase in backgate-device conductivity takes place. As a result, the backgate potential is able to modulate the channel-substrate depletion layer, and, thereby, modulate the MESFET source-drain current. This increase in backgate current is believed to correspond to the trap-fill-limited voltage at which point space charge limited conduction takes place [4,5].

As in the case of ion implanted GaAs, high device packing densities are required to optimize the performance of integrated circuits based on MODFET technology; therefore, a knowledge of the magnitude of backgating, the mechanism and limitations involved is essential. Arnold et al. [6] modeled backgating in MODFETs as being dependent on the thickness of the buffer layer and the potential at the buffer-substrate interface. In our investigations, the magnitude of the backgating effect in AlGaAs MODFETs was characterized and related to the device structure and the electrical properties of the buffer layer. An insight into the mechanism involved was determined from examination of MODFET transconductance and long-gate capacitance dependence on backgate voltage and the characteristics of the backgate leakage current.

The material used for MODFET fabrication consisted of SI GaAs substrates on which the following sequence of layers were grown by MBE: 0.9 μm GaAs buffer (lightly p-type), 25 Å undoped $Al_{0.3}Ga_{0.7}As$ spacer, 380 Å Si doped $Al_{0.3}Ga_{0.7}As$ ($n = 1.6 \times 10^{18} cm^{-3}$), and 410 Å Si doped GaAs contact layer ($n = 1.6 \times 10^{18} cm^{-3}$). Fabrication proceeded as follows: First, device areas were isolated by a 0.15 μm chemical mesa etch. Ohmic contacts were then formed by sequential E-beam deposition of layers of Au, Ge, and Ni, followed by alloying at 425°C for 30 seconds. Gate recess etching, using a $3NH_4OH:1H_2O_2:1000H_2O$ solution, was used to

determine the mode of device operation. The gate metalization consisted of sequentially deposited Cr/Pd/Au. The two types of MODFET-backgate structures investigated and the circuit configurations employed are shown schematically in Figure 3.1. The mesa isolated ohmic backgate contacts are referred to as sidegate (SG) or endgate (EG) depending upon their location.

The effect of negative sidegate voltages on the saturated drain current, I_{DDS} at V_D = 1.0 V of a representative 2 μm gate E-mode MODFET, is shown in Figure 3.2. The zero threshold voltage for the onset of backgating is indicative of a trap-free buffer layer. The corresponding sidegate current, I_{SG}, is also shown in Figure 3.2. These sidegate characteristics resembled closely those of a reverse biased gate contact on the p-type buffer layer. In the case of isolated source and drain ohmic contacts, formed only on the heterostructure, the reverse bias leakage current was several orders of magnitude lower than for gate contacts on the buffer layer. This indicates that a higher barrier, n-p junction, exists between the ohmic contact metallization and the buffer layer. Consequently, the high level of sidegate current measured is attributed to leakage through the gate metallization-buffer layer contact and the considerably lower resistivity of the high purity p-type buffer layer ($\sim 2 \times 10^6$ Ω/□) compared with high quality undoped SI GaAs substrates. Similar sidegate leakage current characteristics were measured for D-mode MODFETs.

The transconductance dependence on gate voltage as a function of sidegate voltage for representative 2 μm gate length E-mode and D-mode MODFETs is shown in Figure 3.3. For the E-mode device (Figure 3.3a) biased at V_D = 1.0 V, negative sidegate voltages produce a transconductance peak shift to higher gate voltages and a reduction in the overall transconductance. A similar effect was observed for D-mode devices, as shown in Figure 3.3b, except that in this case the transconductance peak shifted to lower negative gate voltages. For both types of device, positive sidegate voltages have little effect on the transconductance chara teristics, which may be attributed to the low leakage current of reverse biased isolated ohmic contacts.

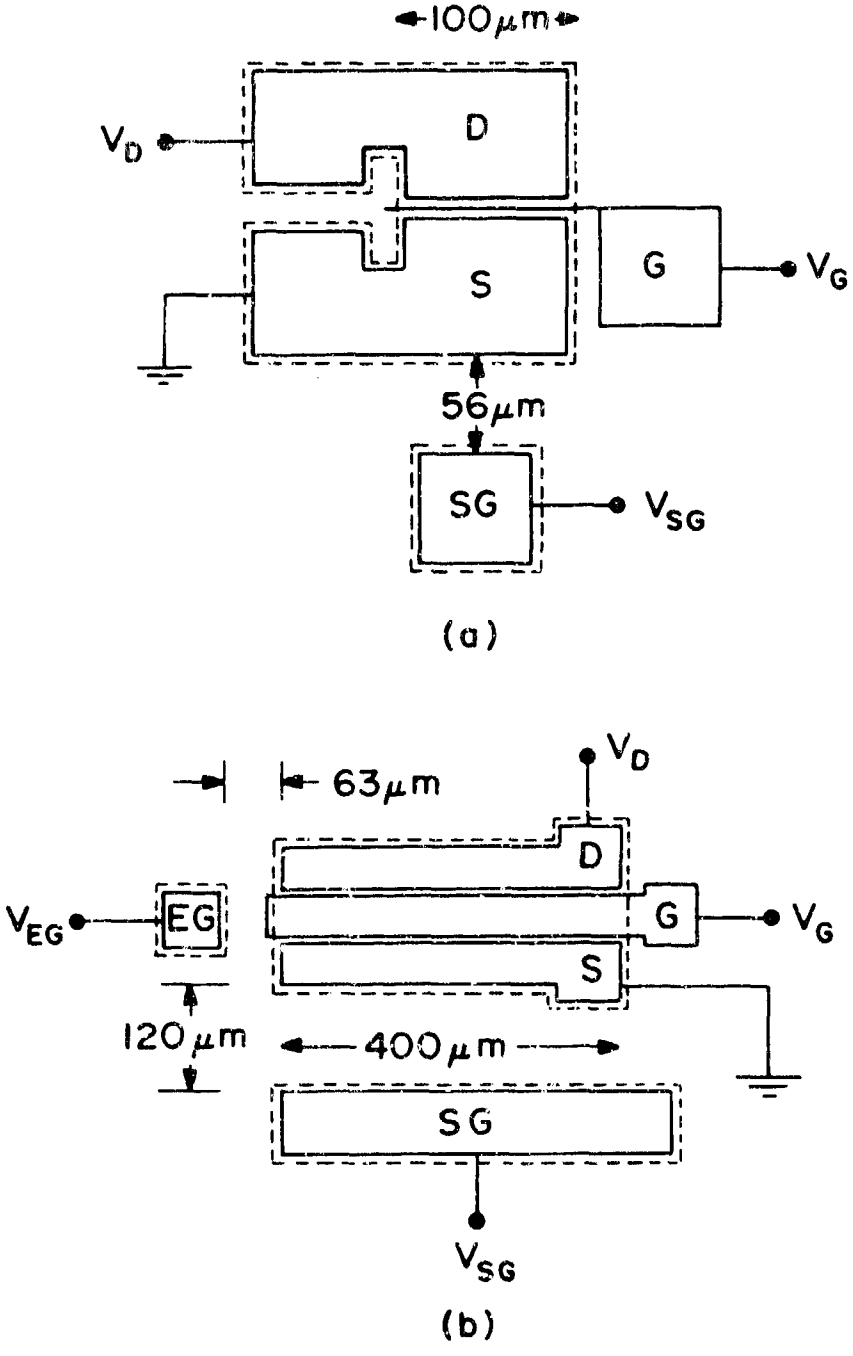


Figure 3.1 Backgating measurement configurations for (a) 2 μm and (b) 50 μm gate length MODFETs. The sidegates in (a) and (b) have dimensions 75 μm x 75 μm and 75 μm x 450 μm, respectively. The endgate in (b) has dimensions 75 μm x 75 μm. Dashed line represents mesa edge.

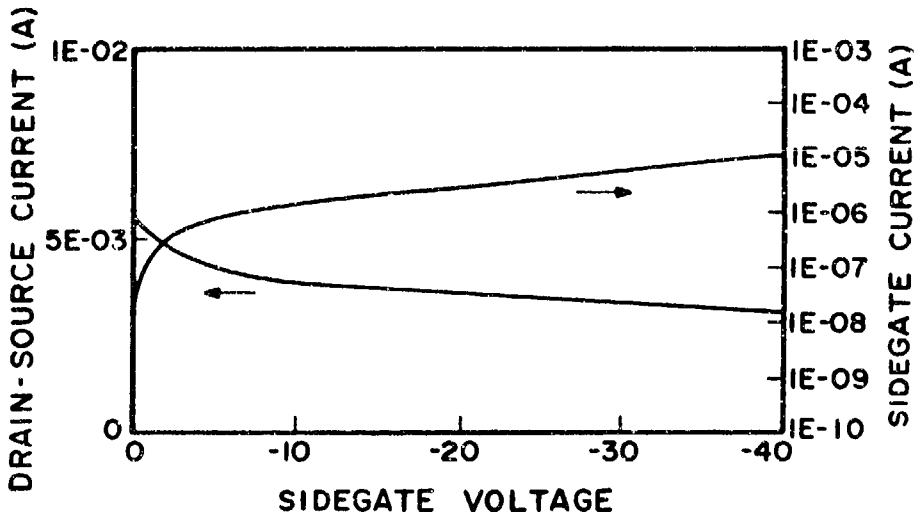
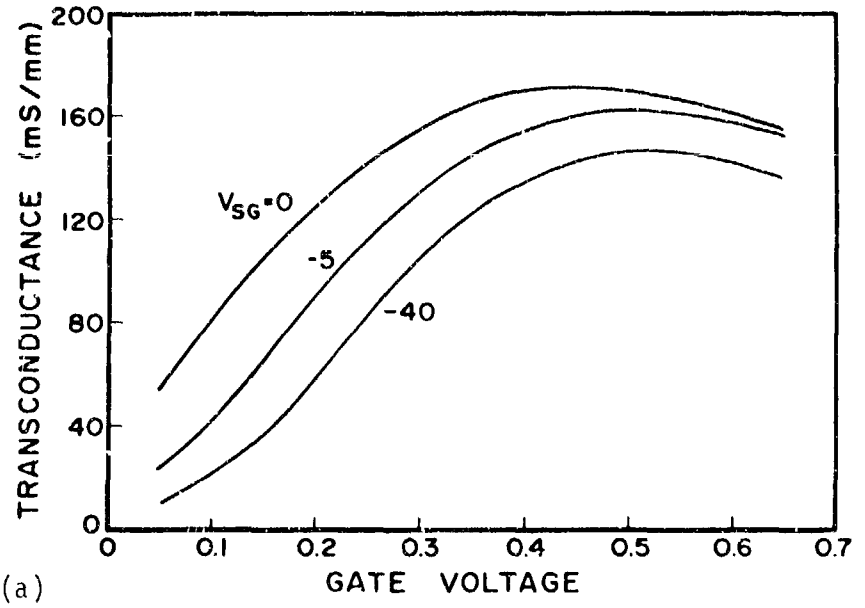
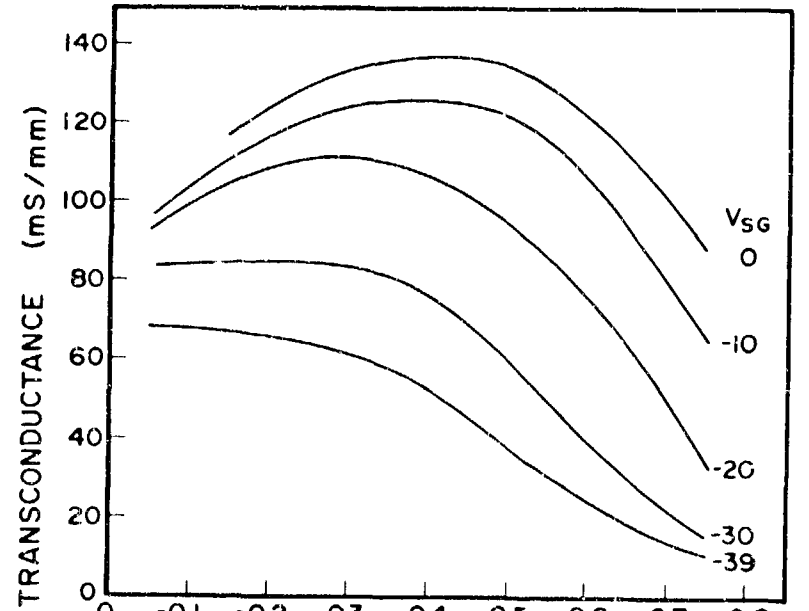


Figure 3.2 Dependence of drain-source current and corresponding sidegate current on sidegate voltage for an E-mode 2 μm gate length MODFET with gate bias V_G = -0.5 V and V_D = 1.0 V.

In order to determine the mechanism involved in the observed sidegating effects, the gate capacitance of 50 μm gate length MODFETs was measured as a function of sidegate and endgate voltage. The results of measurements on representative E-mode and D-mode devices, carried out at a frequency of 1 MHz, are shown in Figure 3.4. For a gate bias of 0.3 V applied to the E-mode device (Figure 3.4a), which corresponds to the "on-state," little change of gate capacitance and, therefore, gate depletion layer is seen up to an endgate threshold voltage of -30 V. For V_G = 0 and -0.3 V, two threshold voltages for modulation of the gate depletion layer are observed at endgate voltages of zero and ≈ -30 V. The zero volt threshold indicates that the gate depletion layer is not isolated and that it extends up to the AlGaAs/GaAs interface. The -30 V threshold corresponds to breakdown of the reverse biased MODFET gate metallization on the GaAs buffer layer. At V_G = -0.3 V, the channel is almost cut off and the gate capacitance is most sensitive to the negative backgate voltage. In this case, some gate capacitance dependence on positive sidegate and endgate voltages is observed. A similar behavior is observed with the sidegate contact; the quantitative differences compared with the endgate results being attributed to a different geometry and location of the backgate contacts. In the case of a

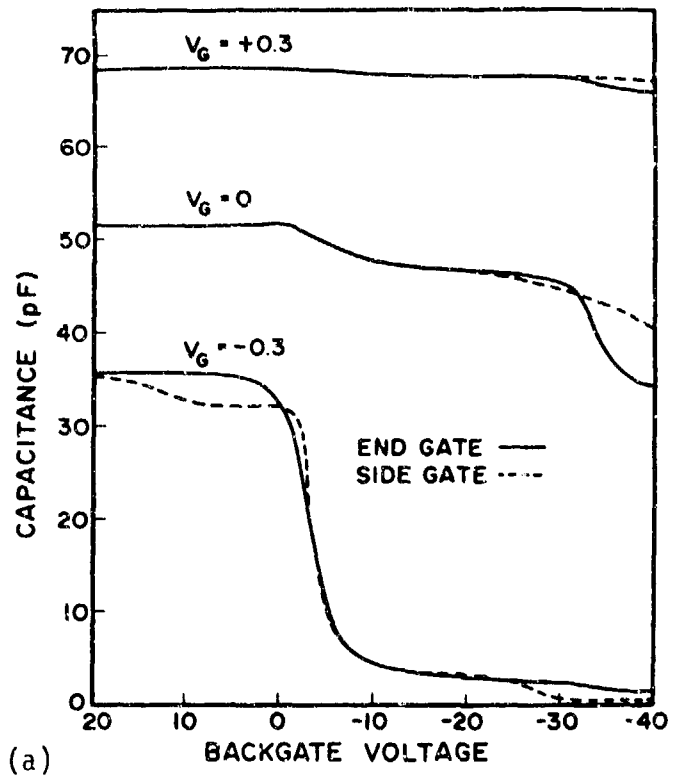


(a)

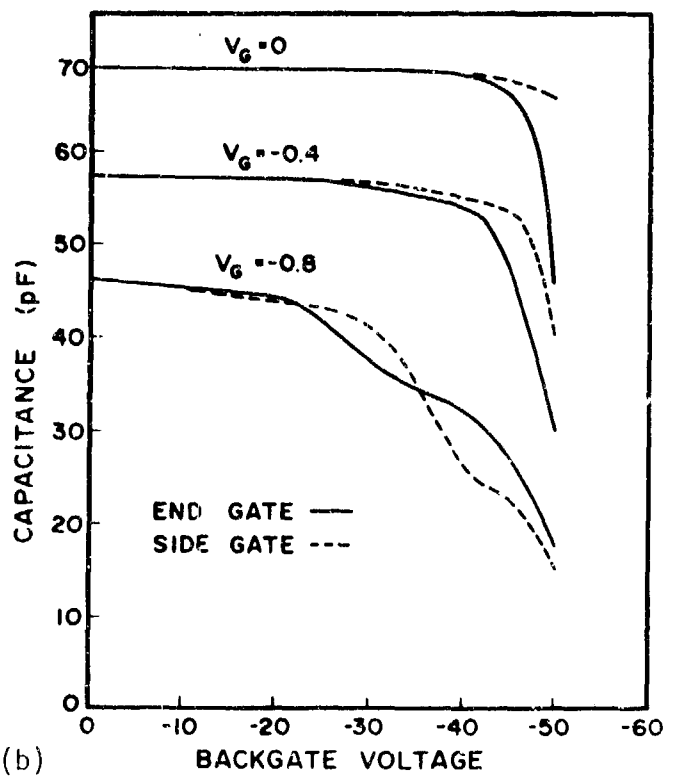


(b)

Figure 3.3 Dependence of transconductance on gate voltage as a function of sidegate voltage for (a) E-mode and (b) D-mode 2 μm gate length MODFETs biased at V_D = 1.0 V.



(a)



(b)

Figure 3.4 Dependence of gate capacitance on backgate voltage for (a) E-mode and (b) D-mode 50 μm gate length MODFETs.

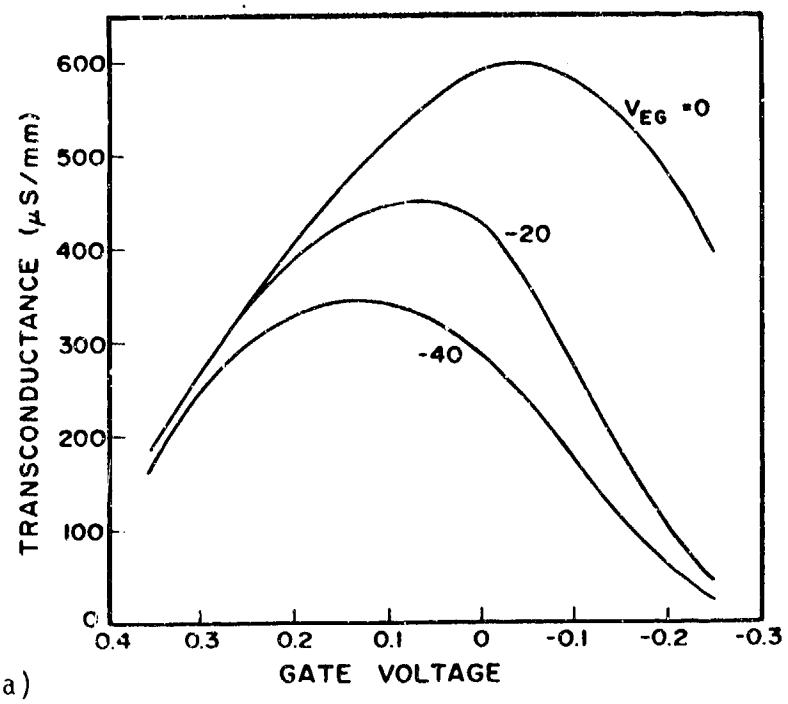
representative D-mode device, qualitatively similar results were observed, as shown in Figure 3.4b.

The transconductance-gate voltage profiles, which are expected to correspond to the capacitance-voltage profiles of the 50 μm gate length MODFETs, are shown in Figure 3.5. Here, the source drain voltage was fixed at 0.02 V for minimal distortion of the gate depletion layer. For the E-mode device (Figure 3.5a), the peak transconductance decreased in magnitude and shifted to lower gate voltages with increasing endgate bias. In this case, an endgate voltage of -40 V produced a ≃ 0.2 V peak shift compared with the zero endgate voltage profile. A similar peak shift toward more positive gate voltages and a reduction in peak transconductance was observed for D-mode devices as shown in Figure 3.5b.

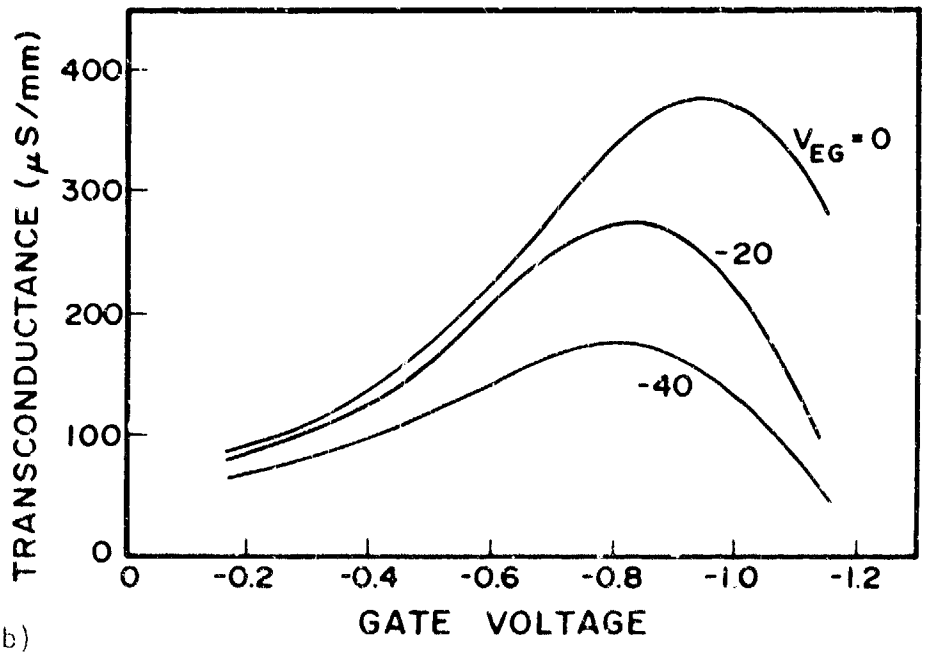
At gate bias voltages where the gate capacitance is independent of the backgate voltage the MODFET current-voltage characteristics still show a significant degree of backgating. The modulation of the transconductance characteristics indicates that negative backgate voltages cause depletion of the 2DEG and extend the carrier depletion in the adjacent doped AlGaAs. Here, the peak transconductance is assumed to correspond to the condition of zero parallel conduction in the AlGaAs and maximum conduction in the 2DEG channel.

However, since the potential profile in the buffer layer under the MODFET metallization is unknown, the precise spatial band adjustment by the backgate voltage and the depletion mechanism of the channel are unknown.

An approach investigated for minimizing backgating in mesa isolated MODFETs was the insertion of a guard ring around the backgate electrode. The two "guard-ring" - backgate structures included in the MODFET mask set are shown in Figure 2.6. In one structure, the guard ring is connected to one of the ohmic electrodes of the type I MODFET and surrounds the "endgate," which is located 15 μm from the MODFET. In the second structure, the guard ring does not make contact with the type I MODFET and could, therefore, be biased independently. The backgate in



(a)



(b)

Figure 3.5 Dependence of transconductance on gate voltage as a function of endgate voltage for (a) E-mode and (b) D-mode 50 μm gate length MODFETs biased at V_D = 0.02 V.

this structure was located 15 μm from the side of the MODFET. In the case of the guard ring at the same potential as the source (ground), the degree of backgating was significantly reduced with the drain-source current I_{DSS} dropping by $\leq$10% at V_{BG} = -10V.

3.2 BACKGATING IN PLANAR ISOLATED MODFETS

In order to increase wafer throughput by decreasing growth time, it is desirable to minimize the undoped GaAs buffer layer thickness. As a consequence, isolation by ion bombardment of such species as O^+, Ar^+, B^+ can be effected all the way through to the semi-insulating substrate. In addition, ion bombardment can be used to place a semi-insulating layer between the gate/probe contacts and the undoped GaAs buffer layer.

Initial investigations were carried out on oxygen implanation for isolation of standard MODFET material. Oxygen was chosen as the ion species since it is known to produce carrier compensation by introducing deep levels in GaAs by doping action as well as by radiation damage. Since implantation isolation would be carried out after ohmic contact fabrication, the implanted regions would not experience processing temperatures greater than 100°C during subsequent processing of devices. Consequently, carrier compensation could be attributed to both doping and residual damage.

The MODFET material used in these investigations had the following structure:

410 Å n^+GaAs ($n = 1.2\times10^{18}$ cm^{-3})
380 Å n^+ AlGaAs ($n = 1.1\times10^{18}$ cm^{-3})
25 Å AlGaAs (undoped)
1 μm GaAs (undoped)

The oxygen implant energy was set at 50 KeV. Doses of 3×10^{12}, 1×10^{13}, and 3×10^{13} cm^{-2} were investigated to determine the optimum isolation parameters. Prior to implantation the material was cleaved

into $(5\ mm)^2$ samples and had indium contacts alloyed at the corners for Van der Pauw type Hall measurements of sheet carrier concentration, mobility, and resistivity. The results of oxygen implantation are shown in the following table:

Dose (cm^{-2})	$N_s(cm^{-2})$	$\mu_s(cm^2/V\ sec)$	$\rho_s(\Omega/\square)$
None	$5.2x10^{12}$	$3.4x10^3$	360
$3x10^{12}$	Mixed conductivity		$4.5x10^6$
$1x10^{13}$	Mixed conductivity		$5.3x10^6$
$3x10^{13}$	Mixed conductivity		$6.5x10^6$

For all doses investigated, the originally n^+ doped heterostructure material was found to undergo complete carrier compensation and had sheet resistivities of approximately the same order of magnitude as measured for 1 μm thick undoped GaAs buffer layers. All the implanted samples exhibited mixed conductivity, the type depending on the Van der Pauw sample electrode polarity. The highest dose implanted material showed the highest overall sheet resistivity. The mixed conductivity may be attributed to the existence of parallel layers of low carrier concentration n- and p-type material, the latter due to the undoped GaAs buffer layer. Consequently, investigations were conducted on the backgating characteristics of planar isolated MODFET structures, as a function of the buffer layer thickness and fabricated device structure.

3.2.1 Material and Device Structure

The structure of the material, grown by Molecular Beam Epitaxy (MBE), used in these investigations is shown in Figure 3.6. A 10- period superlattice of 40 Å $Al_{0.3}Ga_{0.7}As$/40 Å GaAs was first grown on Cr-doped substrates to inhibit out diffusion of defects and impurities. An undoped GaAs buffer layer (p^-) was then grown, followed by 25 to 28 Å undoped $Al_{0.3}Ga_{0.7}As$, 400-440 Å n^+ $Al_{0.3}Ga_{0.7}As$, and 400-440 Å n^+GaAs. For the three material structures investigated, identified as A, B, and C, the corresponding buffer layer thicknesses were 1, 0.2, and

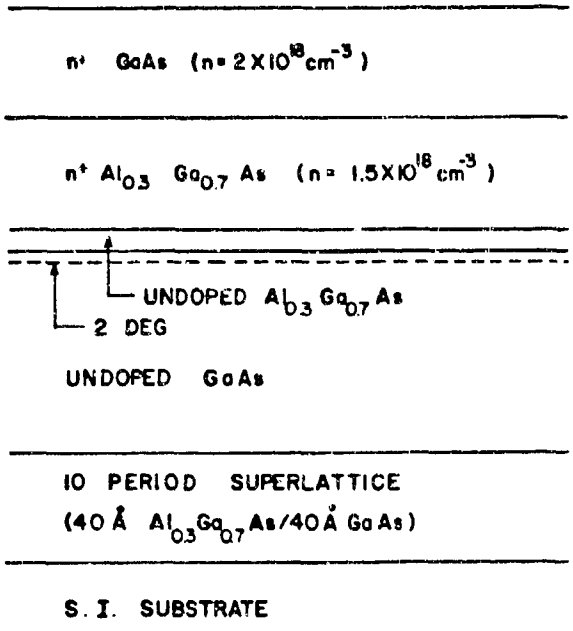


Figure 3.6 Material structure used in these investigations for MODFET fabrication.

0.05 μm. The 300°K sheet mobilities of the wafers (n^+ layer etched off) lay in the range 6100 to 6500 cm^2/V sec with sheet carrier concentrations of $9.2x10^{11}$ to $1.4x10^{12}$ cm^{-2}. The corresponding 77°K sheet mobilities and carrier concentrations lay between the ranges of 63,000 to 79,000 cm^2/V sec, and $9.4x10^{11}$ to $9.9x10^{11}$ cm^{-2}, respectively.

MODFET structures were fabricated on wafers A, B, and C by first forming ohmic contacts. Isolation was then carried out by oxygen implantation using dual doses of $3x10^{12}$ and $6x10^{12}$ cm^2 at respective energies of 50 and 150 KeV. Cr/Pd/Au gates were then deposited after a gate recess and finally, interconnect lines and probe contacts were formed by another Cr/Pd/Au deposition. The above oxygen implantation parameters were chosen in order that the combined theoretical LSS distribution [7] extended into the semi-insulating substrate for material structures with 0.2 and 0.05 μm undoped GaAs buffer layers. In the case of material A, the oxygen implants would be expected to penetrate approximately half-way into the undoped GaAs buffer layer. Although excellent carrier compensation of n^+ AlGaAs is obtained by the low dose oxygen implants, the effect on undoped GaAs

(p^-) and undoped GaAs/AlGaAs superlattices has not been fully characterized.

Shown schematically in Figure 3.7, are the two types of MODFET structures fabricated in these investigations for determining the extent of backgating of the different material structures. In structure I, the implantation mask completely overlaps the ohmic contacts of both the MODFET and the backgate, leaving a 2 μm unisolated border around the outer edges of the contact metallization. In structure II, the isolation implantation mask leaves a 2 μm border around the outer edge of the contact metallization, which is subsequently implanted with oxygen ions. Although the ohmic metallization, as deposited, was ~2700 Å thick, some penetration by oxygen ions in the unmasked contact region is expected to take place. However, the degree of carrier compensation due to oxygen ions which penetrated under the contact is unknown.

A number of structures were investigated where the backgates, referred to here as endgates (EG), were separated from the "end" of the MODFET by distances (x) ranging from 4 to 40 μm. For x = 4 μm, the distance from the end of the gate to the isolated endgate edge was 2 μm. In all cases, the probe pads (area 75x75 μm^2) were spaced 50 μm apart, with the MODFET and endgate located in a central position. The measured maximum extrinsic transconductances for the 1.35 μm gate length MODFETs were typically ~ 220 ms/mm for material A and ~ 150 ms/mm for materials B and C. The lower transconductance for materials B and C is believed to be due to the lower quality of the active device layers after the growth of thin buffer layers, although this was not reflected in the Hall measurements. Under normal device biasing conditions, recent work suggests that a considerable fraction of charge transport occurs deeper than the AlGaAs/GaAs interface [8,9]. In the thin buffer layer structures used in this study, conduction is expected to take place throughout the undoped GaAs, and possibly, in the superlattice which may contain a significant number of electron traps. Some observed I-V characteristic hysteresis and light sensitivity of structure B and C MODFETs attest to the deep conduction mechanism.

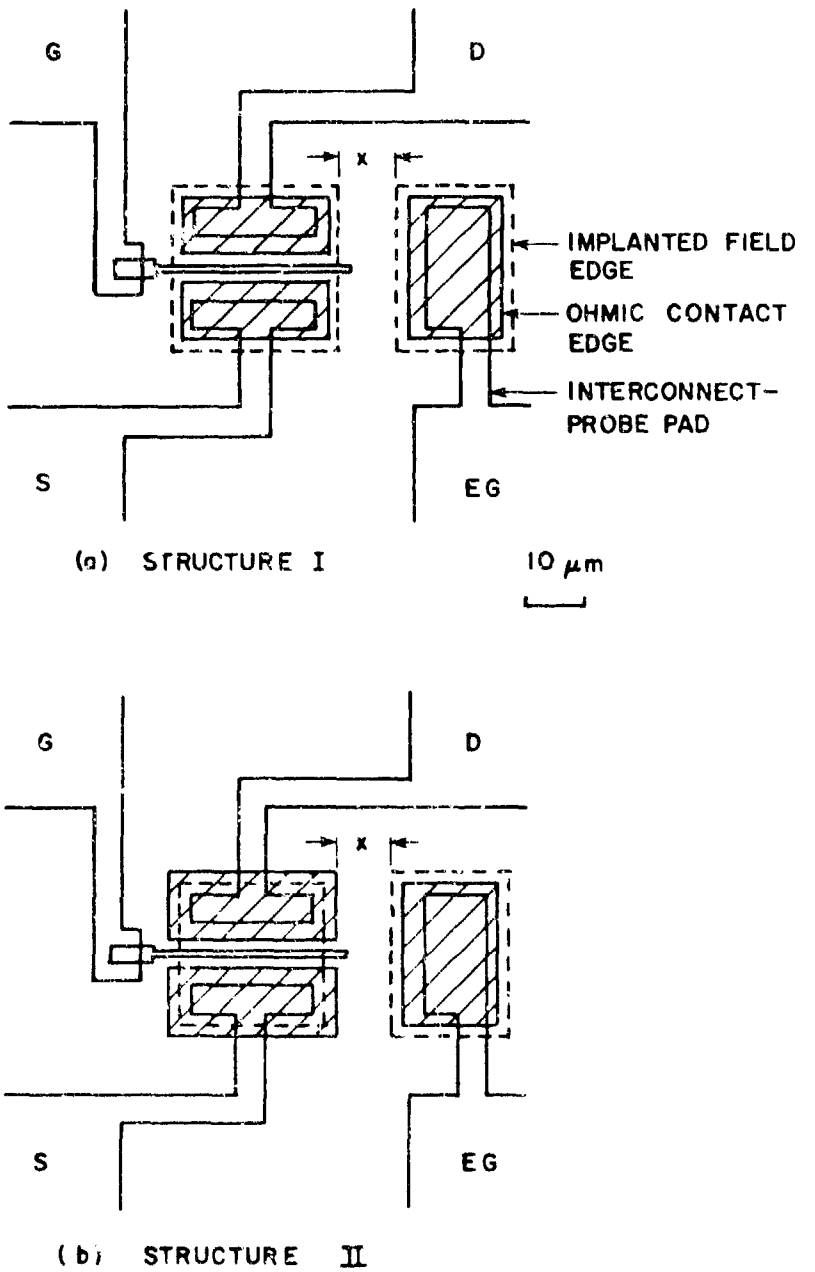


Figure 3.7 Schematic diagrams of the two MODFET and endgate configurations investigated. The hashed areas are covered by ohmic contacts. The region outside the areas bordered by the dashed lines were implanted with oxygen ions.

3.2.2 Results and Discussion

The dependence of MODFET I_{DDS} on endgate voltage for material A is shown in Figure 3.8. For ease of comparison between different structures, I_{DDS} was normalized with respect to the current at zero endgate voltage. In this case and all other structures investigated, the results are representative for I_{DDS} values of ~ 2 mA at zero endgate voltage. Backgating measurements were carried out at drain and gate voltages of 2.0 and 0.5 V, respectively, with the source connected to ground. The endgate characteristics for 1 μm thick buffer layer structures were quantitatively similar for all x values investigated and, therefore, only representative characteristics for x = 10 μm are shown in Figure 3.8. The corresponding full transistor characteristics at endgate voltages of 0 and -5 V are shown in Figure 3.9. Similar results were also obtained for structure II devices. In both cases, for negative endgate voltages, a zero threshold voltage for I_{DDS} decay was observed. Here, I_{DDS} dropped by ~ 25% at V_{EB} = -10 V, but little I_{DDS} modulation was observed for positive endgate voltages.

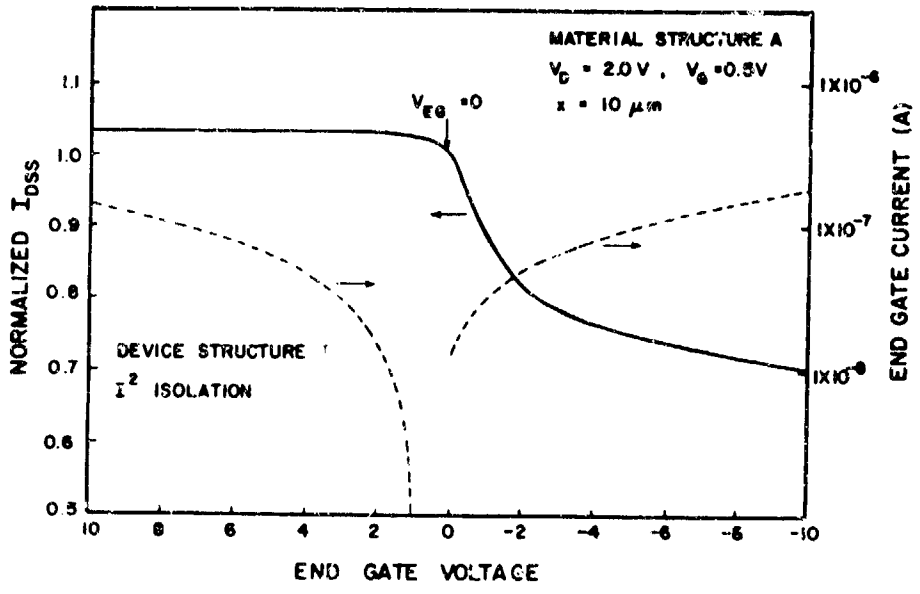
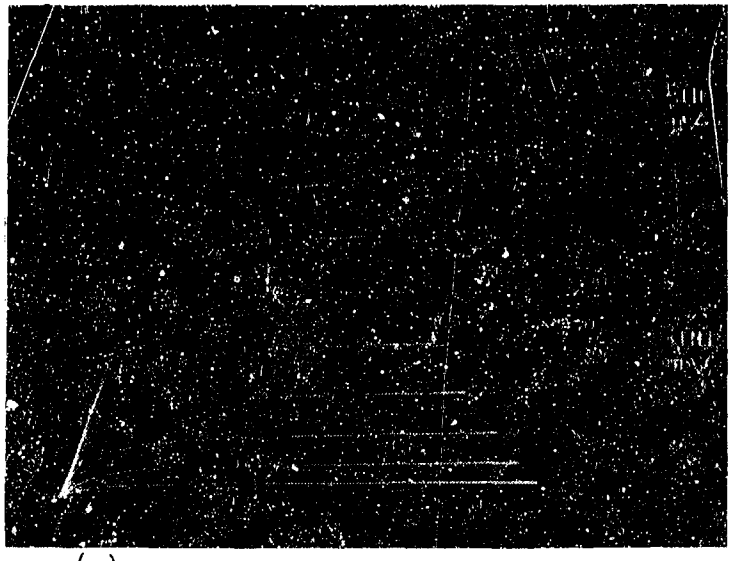
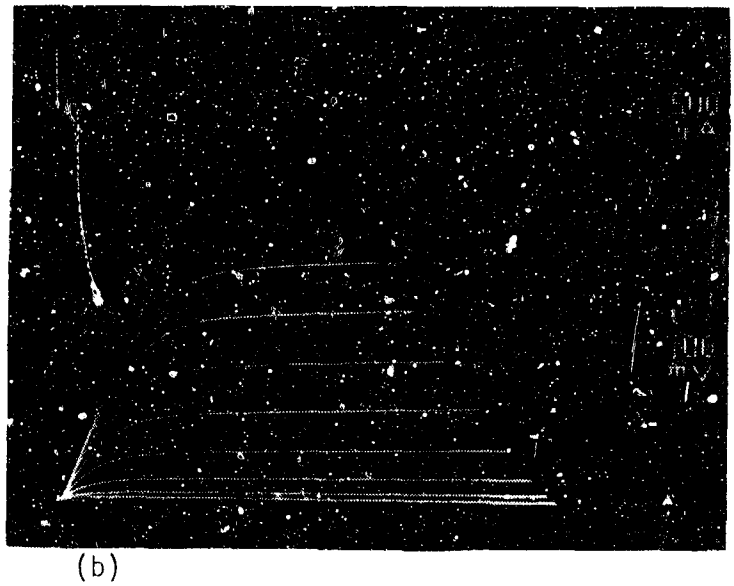


Figure 3.8 Endgating characteristics of MODFET structure I on material A with endgate-MODFET separation x = 10 μm.



(a)



(b)

Figure 3.9 Type I E-mode MODFET characteristics at endgate voltages of (a) 0 V and (b) -5 V. The gate bias voltage step is 100 mV.

The endgate leakage current dependence on positive and negative endgate voltages, shown in Figure 3.8, is characteristic of reverse biased rectifying junctions, which include both the MODFET endgate and probe-pad interfaces with the GaAs buffer layer. For negative endgate voltages, the MODFET/p^- buffer layer and endgate/p^- buffer layer interfaces are reverse and forward biased, respectively. The opposite biasing sense occurs for positive endgate voltages. In the case of the MODFET and endgate, leakage current may enter the GaAs buffer layer directly, whereas for the probe-pad it has to pass through the oxygen implanted layer. Current leakage may also occur on the unpassivated semiconductor surface, and in the implanted buffer and superlattice layers, although the exact current flow pattern is uncertain. The asymmetry in the endgate leakage current-voltage characteristics near $V_{EG} = 0$ is attributed to the MODFET bias voltages off-setting the endgate voltages. In addition, no significant endgate leakage current dependence on endgate spacing was found. The endgate leakage current for the planar isolated structures was found to be approximately one order of magnitude lower than for mesa isolated structures which attests to the current blocking characteristics of the implanted layer. The minimal endgating characteristic dependence on endgate-MODFET spacing indicates that the voltage distribution near the MODFET active layer is determined by the space-charge distributions of the MODFET-buffer and endgate-buffer layer interfaces, rather than the resistivity of the buffer layer itself, which is relatively conductive compared with the semi-insulating substrate.

In order to determine the effect of the buffer layer thickness on endgating characteristics, further measurements were carried out on structures fabricated on materials B and C. For the case of structure I devices on material B (2000 Å buffer layer), with negatively biased endgates a distinct I_{DSS} modulation dependence on endgate spacing was observed, as shown in Figure 3.10. Increased I_{DSS} modulation compared with material A devices was also observed for positive endgate voltages. However, the endgate leakage current characteristics, with both positive and negative endgate voltages, were quantitatively very similar to those observed for material structure A, and again, little leakage current dependence on endgate spacing was observed. These results suggest that

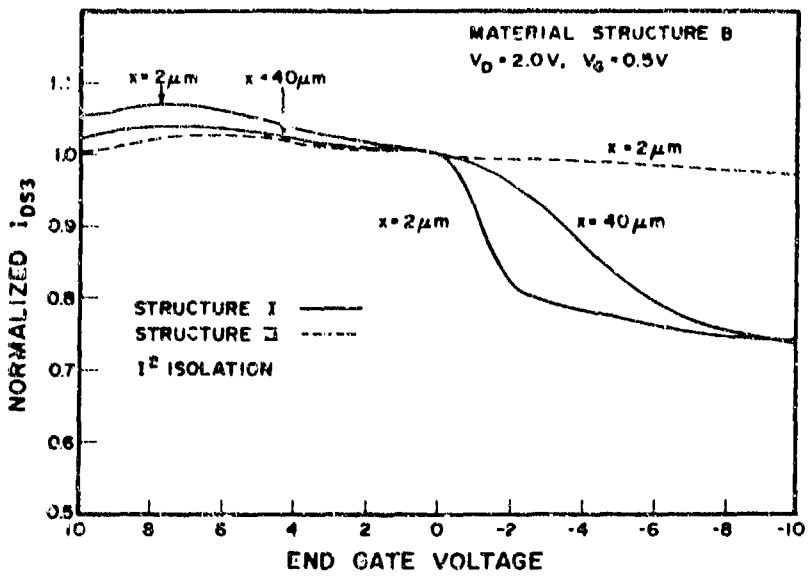


Figure 3.10 Endgating characteristics of MODFET structures I and II on material B.

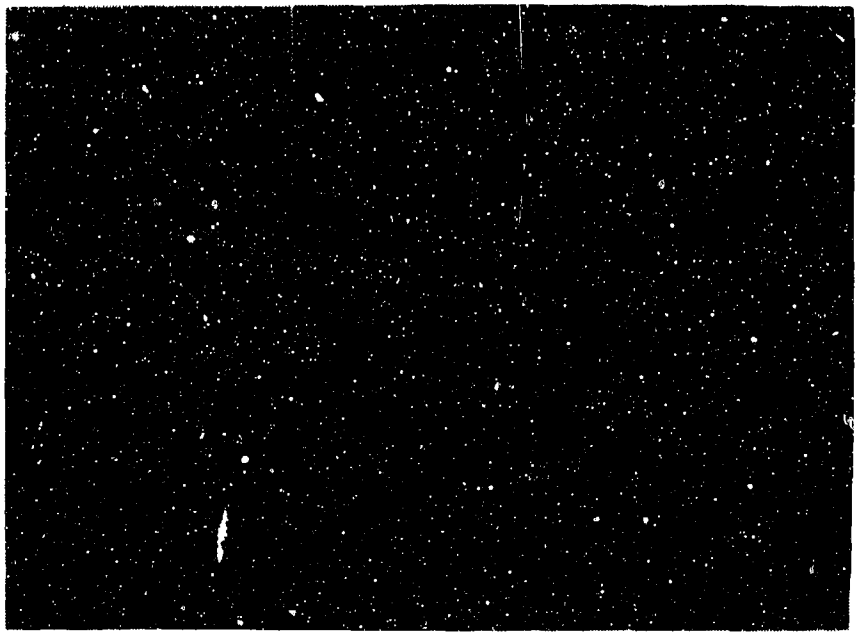
the thin GaAs buffer layer modifies the potential distribution in the vicinity of the MODFET active layer, compared with the 1 μm buffer layer structure, in such a way that it is endgate spacing dependent, while the overall magnitude of leakage current is still dependent on the resistivities of the MODFET, endgate, and probe-pad interfaces with the buffer layer. This also implies that the oxygen implanted GaAs buffer and superlattice layers are still considerably more conductive than the MODFET endgate and the probe-pad interfaces with the buffer layer.

In the case of structure II devices, however, very little endgating was observed for both positive and negative endgate voltages, while the leakage current characteristics were similar to those of structure I devices. Here I_{DDS} was found to drop by $\leq$ 3% when -10 V was applied to the endgate located 2 μm (x = 4 μm) from the MODFET. Lower I_{DDS} modulation was observed for larger endgate spacings. The substantial difference between the engating characteristics of structure I and II devices is a clear indication that the device boundary geometry and associated potential distributions are important factors in determining the degree of isolation of thin buffer layer MODFETs. In structure II devices, it is believed that the source and drain ohmic contacts, which

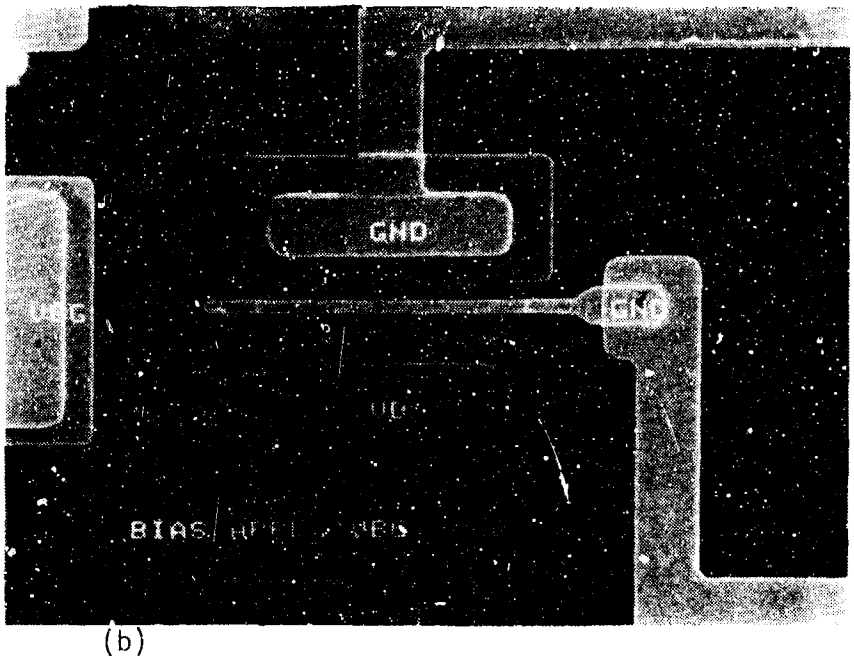
extend beyond the end of the MODFET active layer, provide a potential screen between the active layer and the endgate voltage. Since no such contact extension exists in structure I devices, most of the endgate voltage appears across the active layer/implanted region interface. Evidence for this was provided by voltage contrast scan electron microscope images of biased MODFET and endgate structures. Representative images for type I and II MODFET structures are shown in Figure 3.11. With source-drain, gate, and endgate voltages of 2, 0, and -10 V, respectively, the resulting SEM micrographs, show a distinct difference between structure I and II devices. For the case of the structure I device, there is a sharp change in voltage contrast at the edge of the O^+ implanted region surrounding the MODFET. Since the unimplanted region is conductive, it assumes a potential distribution (dark) consistent with the applied MODFET biases. However, the uniformity of the negative potential (bright) between the MODFET and the endgate shows that most of the endgate voltage appears across the interface between the implanted and unimplanted regions of the MODFET. This implies that in the lateral direction, the negative potential, due to the endgate voltage appears very close to the active channel region.

In the case of the structure II device, no such sharp change in voltage contrast is observed at the edge of the active layer. However, for this structure, the active layer edge is inset 2 μm from the source-drain contact ends. This configuration appears to screen the active layer and, consequently, there is a gradual transition from the voltage of the active region to the negative voltage of the endgate. Consequently, the negative potential of the endgate is located several microns from the active channel region.

For MODFETs fabricated on material with 500 Å buffer layer (structure C), again, a substantial reduction in endgating was observed for structure II devices compared with structure I devices. As shown in Figure 3.12, drain-source current collapse was measured at endgate spacing dependent threshold voltages, which, in general, were lower for structure I devices. The current collapse is similar to that observed in ion-implanted GaAs MESFETs, and is believed to occur at the onset of



(a)



(b)

Figure 3.11 Voltage contrast SEM micrographs of (a) type I and (b) type II MODFET-endgate structures under bias.

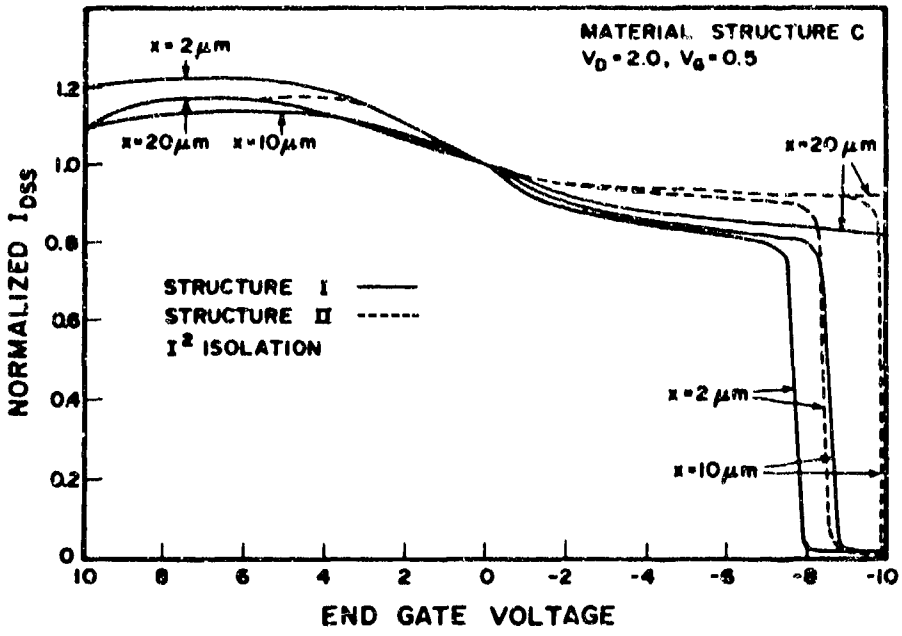


Figure 3.12 Endgating characteristics of MODFET structures I and II on material C.

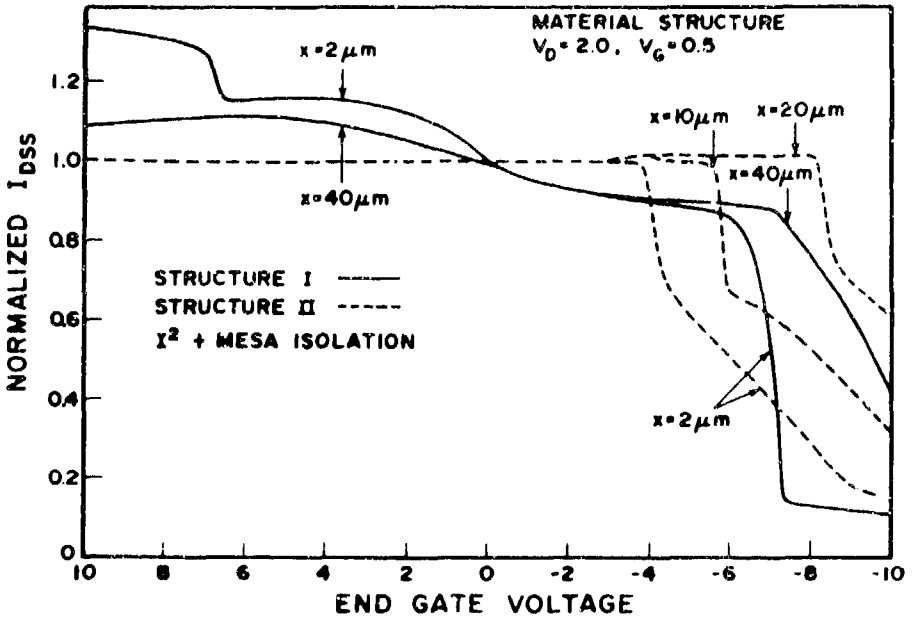


Figure 3.13 Endgating characteristics of MODFET structures I and II on material C after additional mesa isolation.

space charge limited injection in the substrate, and possibly in the superlattice. This effect indicates that the electric field in the semi-insulating substrate and the superlattice, due to the applied endgate voltage, is considerably greater for material structure C than for structures A and B which showed no drain-source current collapse.

Endgate leakage current measurements, however, revealed that there existed no significant threshold voltage for sudden leakage current rises in the bias range investigated, and the leakage current characteristics were quantitatively similar to those of material structures A and B. This observation, again, suggests that the magnitude of the endgate leakage current is independent of the conductivity of the implanted buffer layer and current leakage in the semi-insulating substrate.

For both structure I and II devices, on material C, significant I_{DDS} modulation was observed when positive endgate voltages were applied. In this case, the MODFET/buffer layer and endgate/buffer layer interfaces are forward and reverse biased, respectively, and, therefore, most of the endgate voltage is expected to appear across the latter interface. Since the buffer layer of material C is relatively thin (500 Å), however, a significant fraction of the endgate voltage is also expected to appear across the buffer and superlattice layers between the MODFET and endgate in contrast with the thicker buffer layer material. Like the case of negative voltages, the presence of a positive voltage in the buffer layer in the vicinity of the MODFET active layer is also expected to modify the 2DEG concentration, and consequently, lead to backgating.

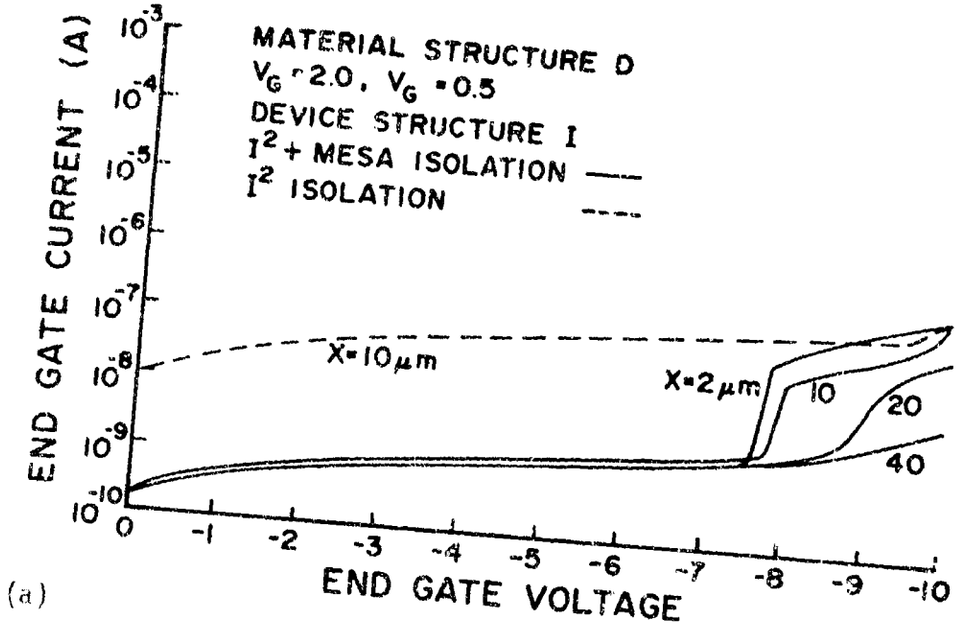
In order to eliminate conduction in the buffer layer and superlattice in the 500 Å buffer layer structure, a mesa etch was carried out on part of the processed wafer, and the backgating characteristics were reevaluated. The mesa depth was ~ 4,500 Å which means that ~ 2,300 Å of the Cr-doped substrate was also etched away. The results of "endgating" measurements on structure I and II devices are shown in Figure 3.13, respectively. For both structure types, lower threshold voltages for I-V collapse were measured although, in general,

the drain-source current falls were softer and more structured than for the planar devices. Again, a significant difference was observed between the backgating characteristics of structure I and II devices. Clearly, the shielding effect of the gate/active layer junction by the source and drain is important, even in the absence of the buffer and superlattice layers between the MODFET and backgate. Although the structure II devices exhibit little drain-source current modulation until a threshold voltage is reached, these threshold voltages are considerably lower for the 2 and 10 μm spacings as compared with structure I devices. Also, a clear threshold voltage dependence on endgate-structure II device spacing is observed, which is analogous to the case of all GaAs, ion implanted devices. If space-charge limited current injection or gate Schottky barrier breakdown is postulated to occur at the current collapse threshold voltage, then the precise nature and magnitude appear to be determined by the boundary conditions.

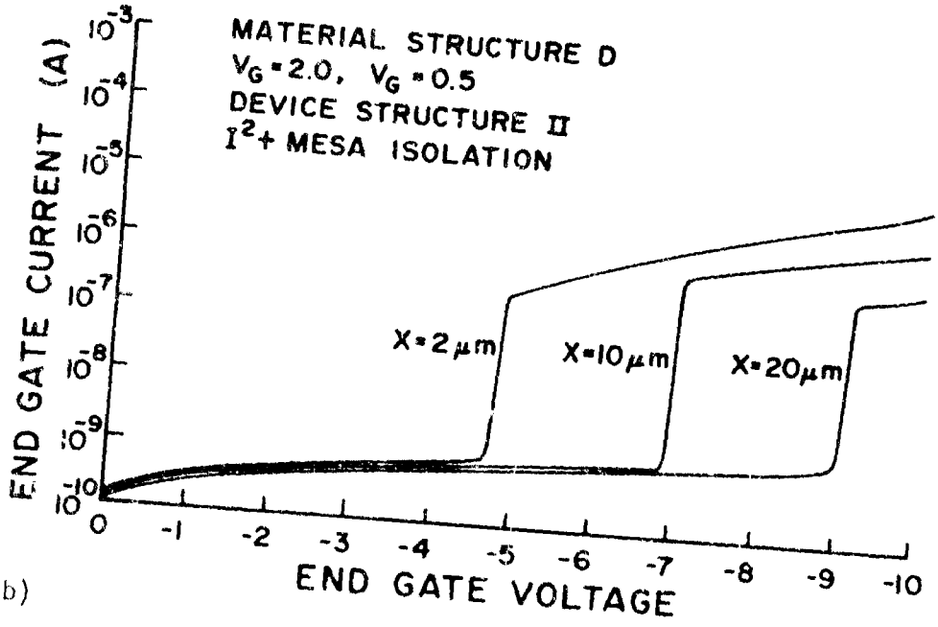
The endgate leakage current characteristics corresponding to structure I and II MODFETs are shown in Figure 3.14. In both types of device up to the point of I_{DSS} collapse, the leakage current is approximately two orders of magnitude lower than for planar devices. These characteristics confirm the conductive nature of the buffer and superlattice layers, even after O^+ implantation, compared with the semi-insulating substrate. At the point of I_{DSS} collapse, the endgate leakage current is observed to rise and then level off at approximately the same order of magnitude as for the planar structures. This endgate leakage current saturation is believed to be due to the current limiting characteristics of the oxygen implanted layer/probe-pad interfaces.

3.2.3 Backgate Voltage Charge Control Model

When a negative voltage is applied to a contact adjacent to a MODFET, a fraction of that voltage appears under the channel, which in turn, leads to band bending in the buffer layer and heterostructure interface region. Here, the voltage under the channel is referred to as the "effective" backgate voltage. In order to determine the effect of the backgate voltage on the electrical properties of the MODFET, it is



(a)



(b)

Figure 3.14 Endgate leakage current characteristics of (a) structure I and (b) structure II MODFETs on material C after an additional mesa etch.

necessary to calculate the two-dimensional electron gas (2DEG) sheet carrier concentration, n_s, as a function of backgate voltage. The saturated drain current, I_{DDS} can then be calculated from the approximate linear relationship between I_{DDS} and n_s. The effect of an applied backgate voltage on the AlGaAs/GaAs heterostructure conduction band edge is shown in Figure 3.15. Calculation of n_s proceeds by solving Poisson's equation for both the GaAs and AlGaAs layers and using charge neutrality to establish the equilibrium condition.

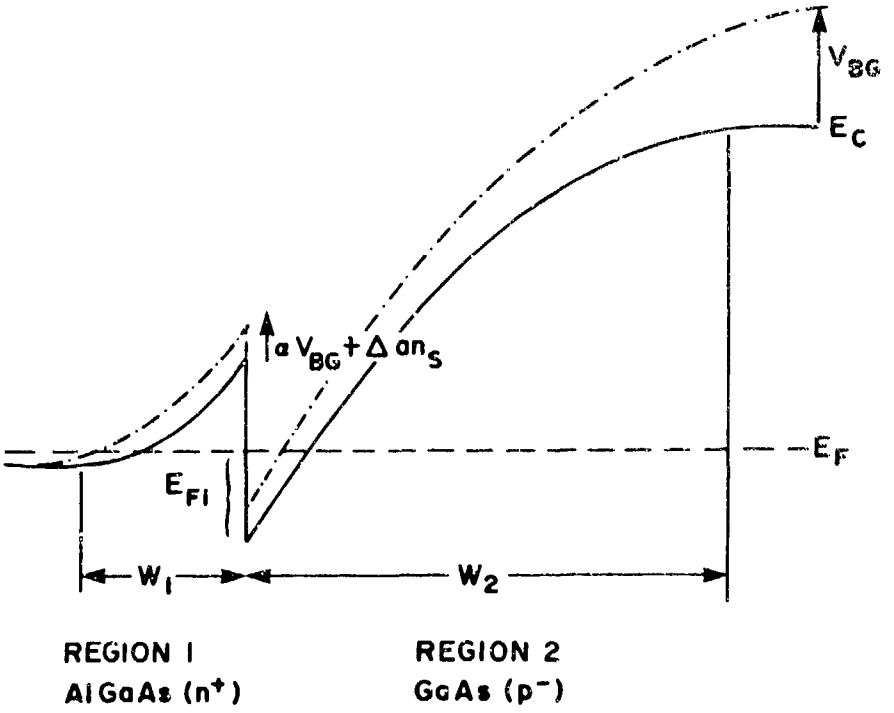


Figure 3.15 Schematic diagram showing the effect of an applied backgate voltage on the MODFET AlGaAs/GaAs heterostructure conduction band edge profile.

3.2.4 Solution of Poisson's Equation for Region 1

For the purposes of simplicity, the effect of the gate is not taken into account. This assumption corresponds to the case of depletion-mode device structures whose backgating characteristics are experimentally similar to those of enhancement-mode devices. Here, the n^+ doped AlGaAs layer is assumed to be sufficiently highly doped so

that the electrostatic potential difference between the conduction band edge and the Fermi level can be ignored.[10]

From Poisson's equation, the electric field in Region 1 is given by

$$E(x) = \frac{dV}{dx} = \frac{q}{\epsilon_1} N_D (x-w_1) \tag{3.1}$$

where ω_1 is the depletion depth. Integrating Eq. (3.1) gives the voltage distribution in Region 1, i.e.,

$$V = -\frac{q}{\epsilon_1} N_D \left(\frac{x^2}{2} - w_1 x\right) \tag{3.2}$$

The depletion depth ω_1 is then given by

$$w_1 = \left(\frac{2\epsilon_1 \phi_B}{N_D}\right)^{1/2} \tag{3.3}$$

where ϕ_B is the electron barrier height.

3.2.5 Solution of Poisson's Equation for Region 2

In Region 2 (lightly p-type), assuming that the electron gas lies in a two-dimensional plane at the interface (x = 0), the electric field is given by

$$E(x) = \frac{dV}{dx} = -\frac{q}{\epsilon_2} N_A (x - w_2) \tag{3.4}$$

Integrating Eq. (3.4) gives the voltage distribution in Region 2, i.e.,

$$V = \int_0^V dV = -\frac{q}{\epsilon_2} N_A \left(\frac{x^2}{2} - w_2 x\right) \tag{3.5}$$

The depletion depth ω_2 is then given by

$$w_2 = \left(\frac{2\epsilon_2 V_B}{qN_A}\right)^{1/2} \tag{3.6}$$

where V_B is hole barrier height. In actual fact, the electron gas is distributed over a finite depth. Therefore, assuming a uniform distribution n over a distance d, the electric field can be expressed in the following form:

$$E(x) = \frac{dV}{dx} = -\frac{q}{\epsilon_2}\int_0^x n\,dx + \frac{q}{\epsilon_2}(n_s + N_A w_2 - N_A x) \tag{3.7}$$

Integrating Eq. (3.7) over the limits x = 0 to ω_2 gives the following expression for ω_2:

$$w_2 = \left[\frac{2e_2}{qN_A}\ (V_B - \beta)\right]^{1/2} \tag{3.8}$$

where $\beta = \frac{qn_s d}{2\epsilon_2}$ (3.9)

For $n_s = 1 \times 10^{12}\,cm^{-2}$, $\epsilon_r = 12.9$ and $d = 100$ Å

$\beta = 0.07$

The same expression for β is obtained if the 2DEG plane is assumed to lie at x = d/2. Consequently, a similar value for β is expected when the precise electron probability function for the quantum well structure is taken into account.

Since V_B is considerably greater than β, the effect of β is ignored in subsequent calculations. Consequently, the expression used for ω_2 is the same as given by Eq. (3.6).

3.2.6 Charge Neutrality Condition

Since the effect of the gate is not taken into account, the equilibrium state can be determined by applying the charge neutrality condition over Regions 1 and 2, i.e.,

$$N_A w_2 + n_s = N_D w_1 \tag{3.10}$$

Substituting for w_1 (Eq. (3.3)) and w_2 (Eq. (3.6)) in Eq. (3.10) gives

$$N_A\left(\frac{2\epsilon_2 V_B}{qN_A}\right)^{1/2} + n_s = N_D\left(\frac{2\epsilon_1 \Phi_B}{qN_D}\right)^{1/2} \tag{3.11}$$

Here, the approximation $\epsilon_1 = \epsilon_2 = \epsilon$ gives

$$n_s = \left(\frac{2\epsilon}{q}\right)^{1/2}\left[(N_D\Phi_B)^{1/2} - (N_A V_B)^{1/2}\right] \tag{3.12}$$

$$\text{where} \quad \Phi_B = \Delta E_C - E_{Fi} + \alpha V_{BG} - \frac{kT}{q} \tag{3.13}$$

$$\text{and} \quad V_B = E_g + V_{BG}(1-\alpha) + E_{Fi} - \frac{kT}{q} - \delta \tag{3.14}$$

where ΔE_C is the conduction band discontinuity, α is an arbitrary backgate voltage division factor, E_{Fi} is the Fermi level voltage measured from the GaAs conduction band edge at the interface and δ is the voltage difference between the Fermi level E_F, and the valence band edge in the p-GaAs.

Since the n^+ AlGaAs is either degenerate or nearly degenerate the non-ideal depletion layer correction term kT/q, derived from Boltzmann statistics for non-degenerate material, should be modified. However, for the case of n^+ doped AlGaAs the value of the correction (> kT/q) is uncertain and since there still remains some ambiguity about the division of the band discontinuity the correction kT/q is retained in these calculations.

For values of n_s between 5×10^{11} and 1.5×10^{12} cm^{-2}, Drummond et al. [11] derived the following approximation for E_{Fi}:

$$E_{Fi} = \Delta E_{Fo}(T) + a.n_s \qquad (3.15)$$

where $a \simeq 0.125\times10^{-12}$ V cm^{-2} and $\Delta E_{Fo} \simeq 0$ at 300°K and $\Delta E_{Fo} \simeq 0.025$ at 77°K and below.

Using the expression $Eg(Al_xGa_{1-x}As) = 1.424 + 1.247x$ [12] and assuming $\Delta E_c = 0.65$ Eg, for x = 0.3 the conduction band discontinuity ΔE_c is calculated to be 0.243 eV. In the calculation of n_s (V_{BG}), the doping levels of N_D and N_A are taken as 1×10^{18} and 1×10^{15} cm^{-3}, respectively. The value of δ used in the calculations is 0.228 eV. Eq. (3.12) can be expressed as a quadratic equation in V_{BG}, the solution of which is plotted in Figure 3.16. The values of α are set arbitrarily at 0 and 1×10^{-3} to obtain a qualitative feel for the influence of this backgate voltage division factor.

The dependence of n_s on V_{BG} is qualitatively similar to that observed for the saturated drain current of fabricated MODFETs with thick buffer layers. Although the calculations do not take two-dimensional geometrical effects into account; the model appears to be accurate, especially since it predicts an extension of the non-gate AlGaAs depletion layer with negative backgate voltage. This effect would result in a shift of the peak transconductance to more positive gate voltages, as has been determined experimentally.

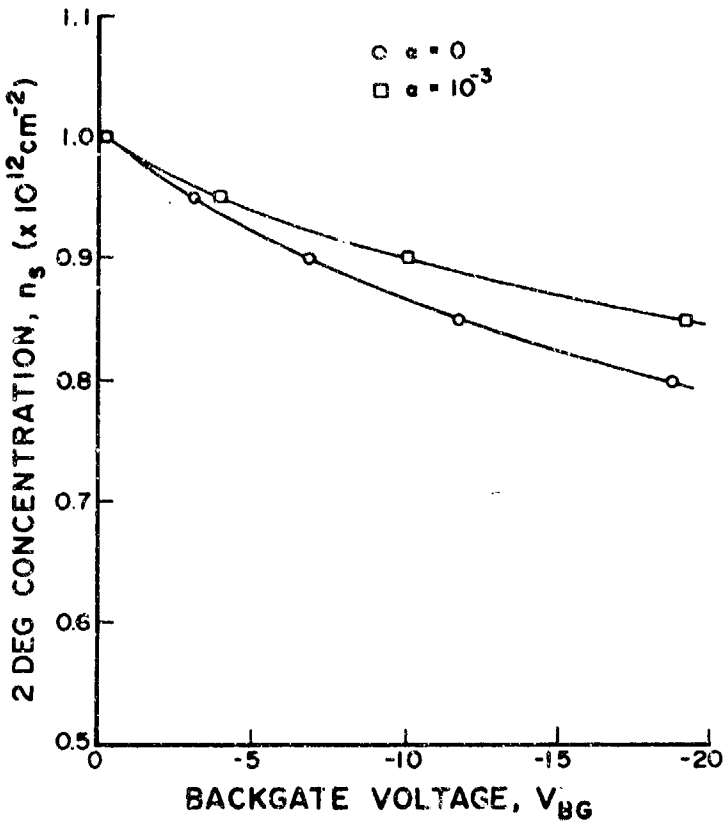


Figure 3.16 The dependence of 2DEG concentration, n_S, on backgate voltage for backgate voltage division factors $\alpha = 0$ and 10^{-3}.

SECTION IV
MODFET OHMIC CONTACTS

4.1 CONVENTIONALLY ANNEALED CONTACTS

4.1.1 TEM Analysis

In order to obtain an insight into the conduction mechanisms of AlGaAs/GaAs MODFET ohmic contacts, it is essential to determine the physical structure of the contact metallurgy itself. Because the conducting layers, consisting of the Two-Dimensional Electron Gas (2DEG), n^+ AlGaAs and n^+ GaAs contact layer, have a combined thickness of typically ≤ 0.1 μm, it is important to use an analytical characterization technique with high resolution. Cross sectional Transmission Electron Microscopy (X-TEM) with its very high lateral and depth resolution offers an attractive technique to examine specific areas of the contact. In addition, this technique provides a powerful failure analysis tool when investigating stressed ohmic contacts. For this purpose, a technique was developed at UES for preparing TEM samples where the specific area of interest was thinned in a controlled manner.

The specimen was first sectioned into 3 x 2 mm^2 rectangular slabs. The slabs were thoroughly cleaned by rinsing with acetone, methanol, and finally blow-dried with nitrogen. Two slabs were glued together face to face using an epoxy resin. Since the epoxy needed to be thermoset under light pressure, two alligator clips were attached to both ends of the glued sample. The glued slabs, held by the alligator clips, were then put on a hot plate, heated to ~50 to 70°C, and left undisturbed for about 6 to 7 hours. After the epoxy was cured, the composite specimen (hereafter called specimen) thus obtained was mounted with crystal bond wax on a 3 cm diameter, 1 cm thick circular glass disk in such a way that the glued faces of the slabs were perpendicular to the surface of the glass disk. Two supporting pieces of silicon (~ 1 x 0.5 cm) were then laid flat on the glass disk on both sides of the specimen. Care was taken to get the specimen and support pieces, which were typically 326 μm thick, evenly seated in the wax. The

specimen was then mechanically thinned to the thickness of the Si support pieces on a lapping wheel using 600 grit sandpaper and flowing water for lubrication. After the specimen was thinned down to the level of the support pieces, mechanical polishing was done using 6 μm followed by 1 μm diamond paste. The polished surface of the specimen had a shiny appearance at this stage. The specimen was then carefully removed by heating the circular glass disk on a hot plate and remounted with the polished side face down. After the wax was hardened, the specimen was thinned to about 40 to 50 μm using the 60 grit sandpaper. The final polishing was done with 6 μm followed by 1 μm diamond paste to smooth out the surface. The mechanically thinned specimen was then carefully removed from the glass disk by soaking in acetone. A copper washer of 3 mm diameter with a 2 mm hole in the center was glued to the specimen. The final thinning was done by ion milling with the specimen rotating under dual ion gun thinning with beams being directed at each side of the sample until a small hole appeared close to the center of the specimen. The system used in this work was a Gatan Dual Ion Mill with 5 KeV Ar^+ ions and a specimen current of 20 μA. A gun tilt of about 15 degrees was also used. No dimpling of the sample was carried out before ion milling.

In order to analyze MODFET ohmic contacts, with particular emphasis on the edge region, sample thinning was focused on TLM patterns used for measuring contact resistance. In this case, the TLM pattern, shown in the basic test structure mask set design in Figure 2.7, was used. The pattern consisted of 75 x 50 μm^2 contact pads with spacings ranging from 2 to 10 μm. The ohmic contact metallization consisted of the sequence 50 Å Ni, 170 Å Ge, 330 Å Au, 150 Å Ni, and 2000 Å Au deposited onto the GaAs cap layer of AlGaAs/GaAs MODFET material.

The approach used here was to employ the thickness of the support pieces as a way of keeping track of the desired region (in this case the contact pads) as a zone of interest during mechanical thinning. Sections of 3 x 2 mm^2 dimension were cut from the patterned wafer in such a way that the gaps between the contact pads were parallel to the 2 mm side (AB) of the chip (see Figure 4.1). The 75 μm sides of the contact pads

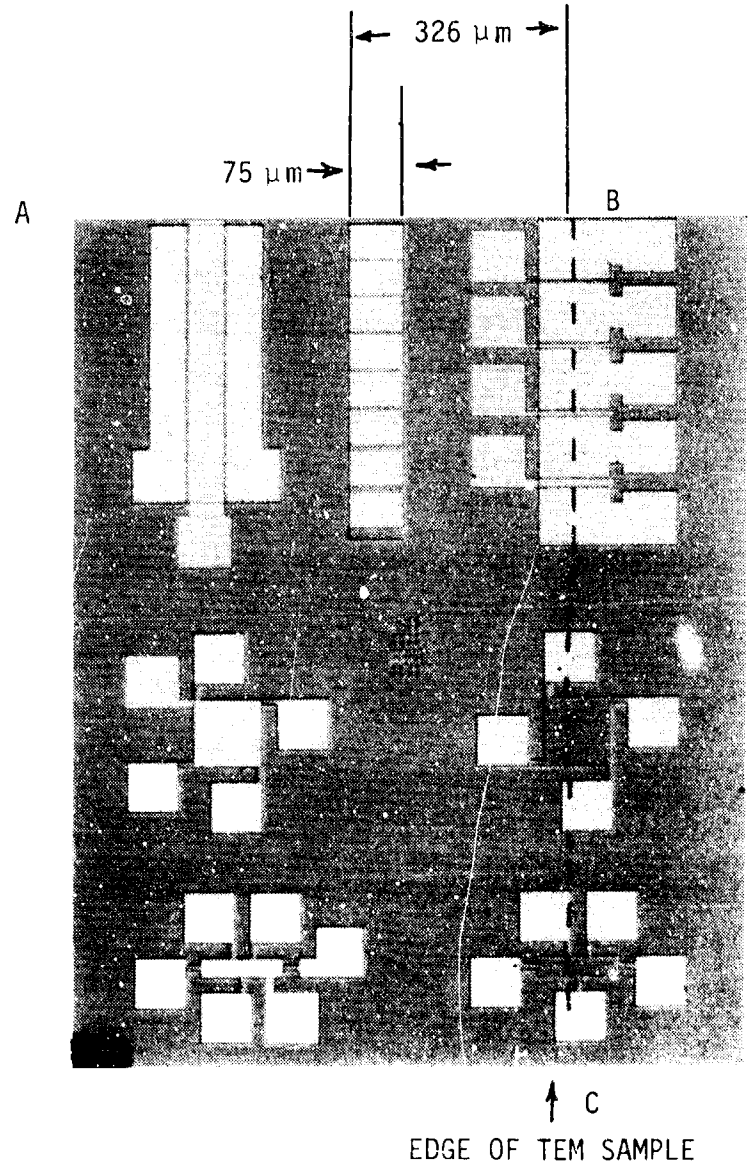


Figure 4.1 Optical micrograph of test structure chip used for TEM sample preparation.

(facing edge AB) were mounted vertically with edge BC in contact with the glass disk and edge AB standing vertically upward. The specimen dimensions were initially cut such that a distance of 326 μm, corresponding to the thickness of the support pieces, existed between the edge (BC) and the upper side of the contact pads. Thus, when the top part of the specimen section was ground down to the silicon support pieces, the top of the sample was aligned with the 50 μm edge of the contact pads. In addition, the sample was cut so that the TLM pattern was positioned centrally to the 3 mm edge. The contact face of one of the device slabs was then glued together with the polished face of a similar 3 x 2 mm^2 slab of blank GaAs using the epoxy resin.

After the initial lapping process, the specimen was examined under an optical microscope. Mechanical thinning with the 600 grit sandpaper was stopped as soon as the metallization of the contact pads and the gaps in between were observed. The processing of the sample was then resumed and lapping from the other side was continued until the contact pads could again be observed. After a small hole had been milled in the sample, the structure was examined by TEM. In order to zone in on a particular part of the contact, additional milling was carried out if necessary.

Figure 4.2(a) shows a low magnification, bright-field micrograph of an entire gap (2.9 μm) of the contact resistance measurement pattern. Extensive contact material penetration is observed in both directions along the <011> axis. Figure 4.2(b) shows a high magnification micrograph of the cross section of an ohmic contact at the edge of the metallization. Lateral penetration of contact material is found to extend ~ 1200 Å away from the contact edge. In this zone, vertical diffusion extends ~ 1300 Å and penetrates well beyond the AlGaAs/undoped GaAs 2DEG interface. Such lateral and vertical penetration of contact material has been found typical for the metallization scheme and alloy cycle employed and is presumably related to the stress generated between the metallization and semiconductor surface during the contacting process. Away from the contact edge, contact metal is generally found to penetrate the n^+ AlGaAs layer

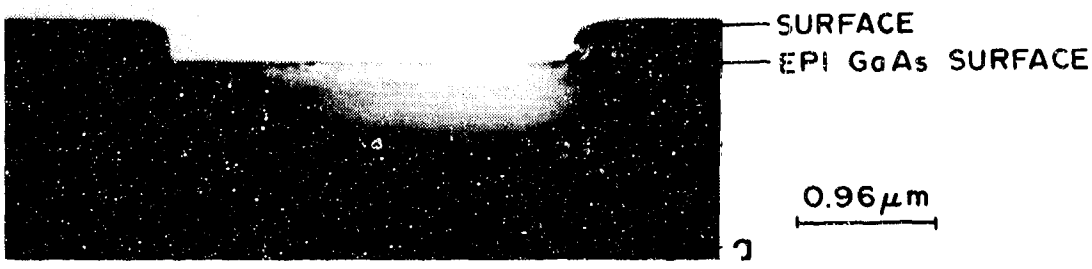


Figure 4.2 Cross section TEM micrographs of: (a) space between two ohmic contacts of the contact resistivity measurement pattern, (b) the edge region of an AlGaAs/GaAs MODFET ohmic contact.

although, apart from a few spike zones, it does not reach the 2DEG interface.

Cross section micrographs of the alloyed region under one of the contact pads are shown in Figure 4.3. The alloyed region extends between 190 Å and 850 Å into the epilayers, from the original metal/GaAs interface, and shows more or less uniform contrast. In a few areas, penetration of the contact material in the form of a vertical spike was observed to a depth of 1250 Å. Dark particles having lateral dimensions ranging from 500 Å to 1860 Å are present at the alloy/GaAs (or AlGaAs) boundary. The original metal/GaAs interface shows lighter contrast than the metal pad or the alloyed region, suggesting the presence of native oxides at the original GaAs surface. This indicates that the alloying process takes place through solid-state interdiffusion, rather than by a melting-regrowth process. This observation is in agreement with the earlier work of Kuan et al [13]. The selected area diffraction pattern shown in Figure 4.4(a) is from the alloyed region and part of the GaAs. In addition to the Bragg diffraction spots due to GaAs in the [110] orientation, many extra spots are visible indicating the formation of other phases. As shown in Figure 4.4(b) some of these extra spots can be indexed on the basis of a hexagonal structure having lattice parameters a = 3.6 Å and b = 5.02 Å. Although these lattice parameters correspond to the NiAs phase, it could also be due to Ni_2GeAs since the two structures are known to have similar lattice parameters [13]. In the light of the fact that Ge is found in the EDS spectrum of the alloyed region, the identification of Ni_2GeAs phase seems to be more reasonable. This region could also be identified as NiAs phase plus Ge. However, as shown in Figure 4.5, the presence of lattice fringes of uniform spacings throughout the alloyed region is indicative of a single phase. Optical diffractogram analysis of the lattice fringes seen in the alloyed region confirms this hypothesis. The fringes can be identified as 2.6 Å (101) type planes of Ni_2GeAs. Optical diffractogram analysis of several regions within the metal pad, such as the one arrowed in Figure 4.5(a), has identified them as γ-(Au-Ge). A higher magnification image of this region is shown in Figure 4.5(b). Regions of this phase have been identified close to the metal/alloy interface.

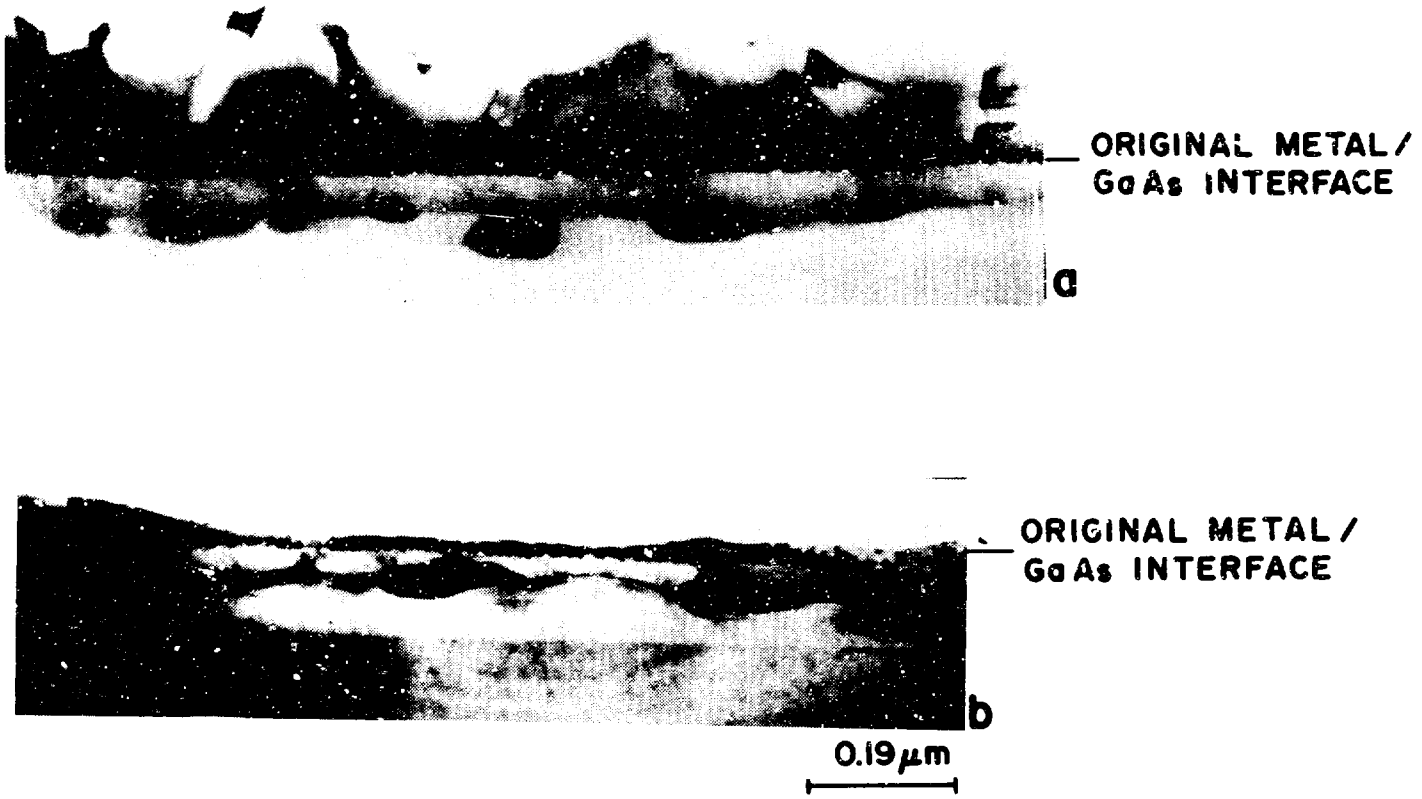
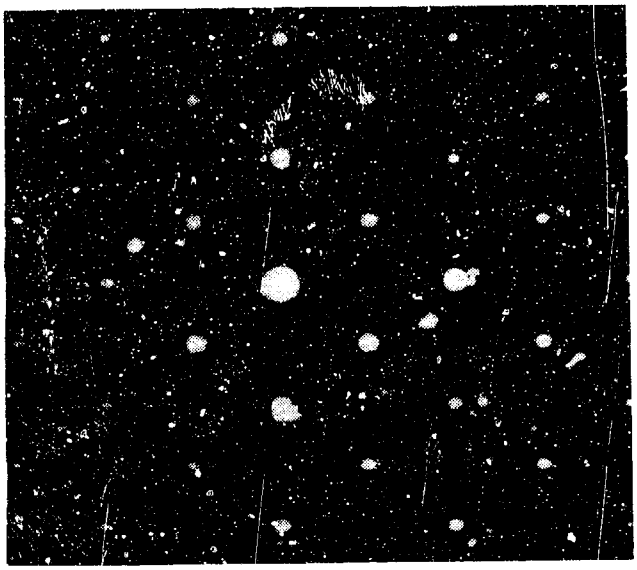
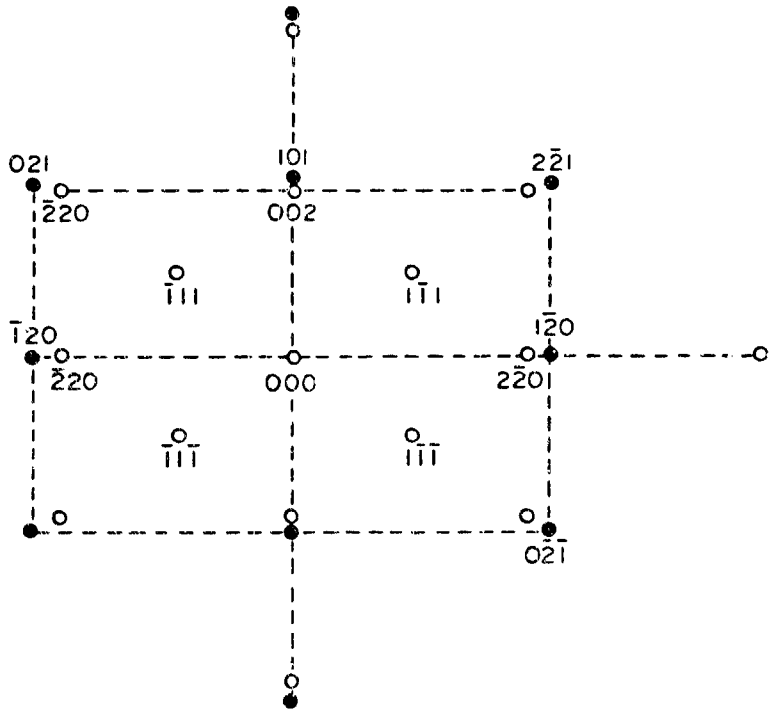


Figure 4.3 Cross sectional bright-field micrographs of the alloyed region under an ohmic contact.

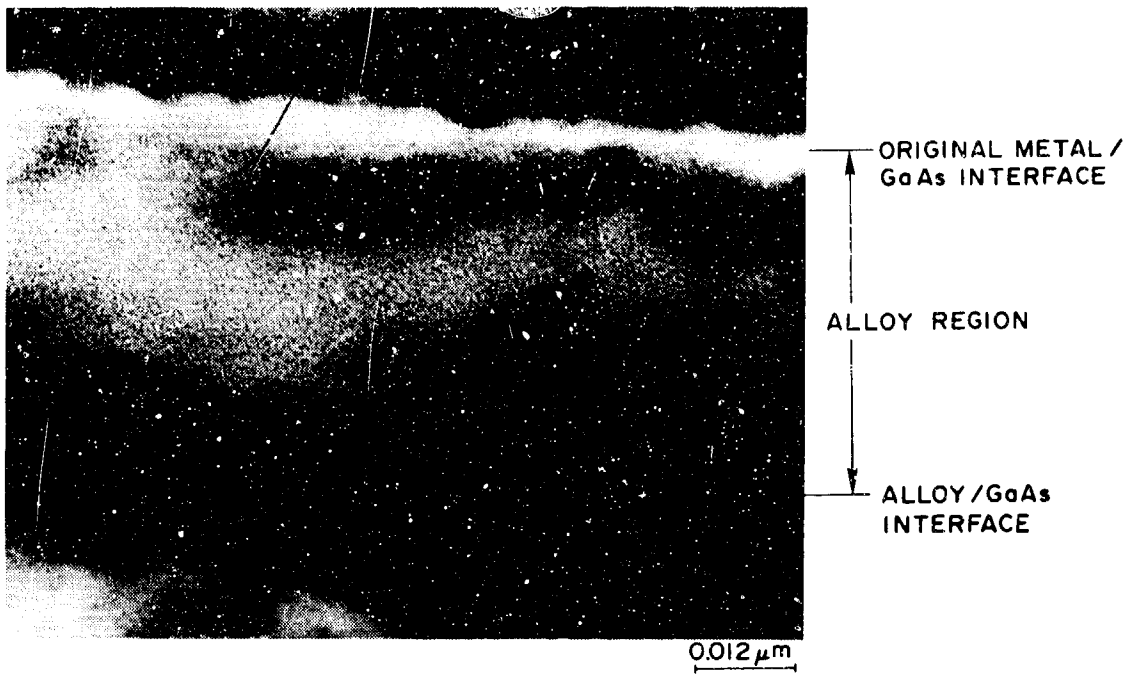


(a)

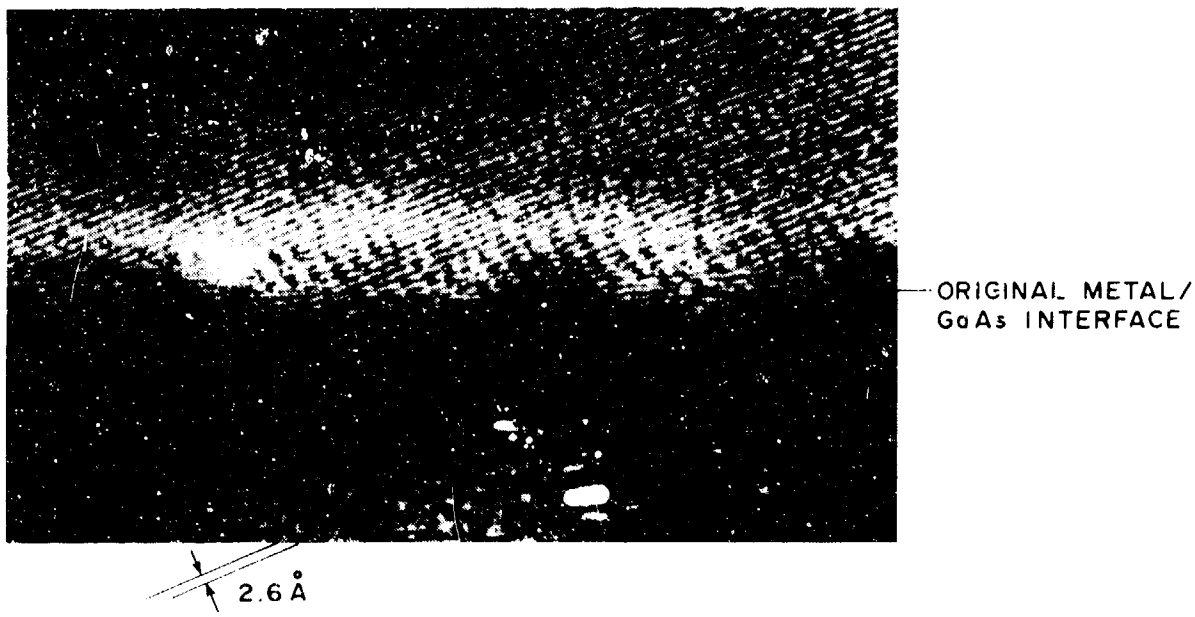


(b)

Figure 4.4 (a) Selected area diffraction pattern of the alloyed region underneath an ohmic contact. (b) Corresponding diagram showing the indexing of Ni_2GeAs and GaAs diffraction patterns (O, GaAs; ●, Ni_2GeAs).



(a)



(b)

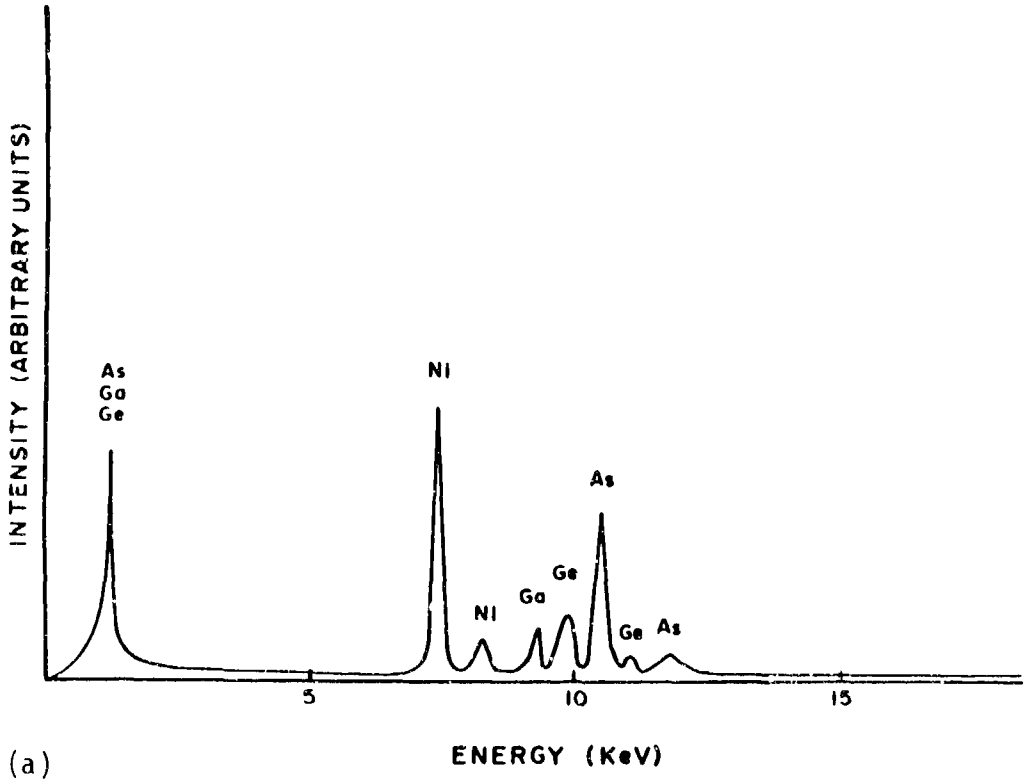
Figure 4.5 (a) Cross sectional high resolution image through the alloyed region. (b) Original metal/GaAs region at higher magnification.

Optical diffractogram analysis of the penetration regions at the gap ends indicates the presence of a number of different phases, including GaAu.

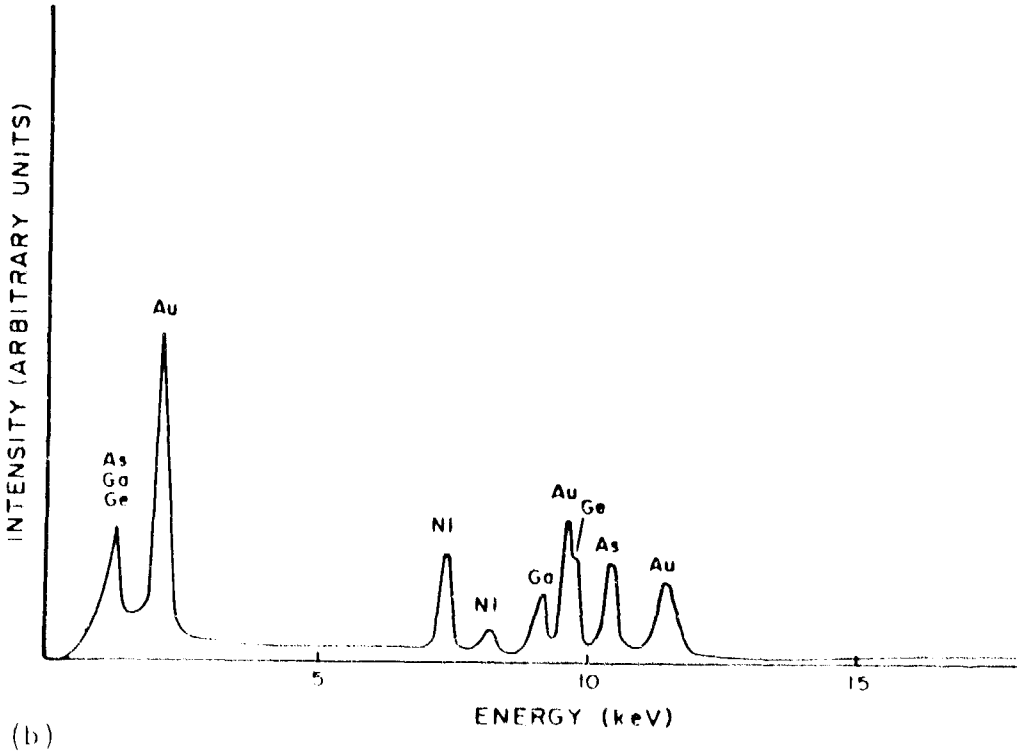
The presence of Ni and Ge throughout the metal/GaAs interfacial regions may be a consequence of the present alloying scheme. From the study of the Ni/GaAs system, Ogawa [14] has shown that Ni easily dissociates a large amount of GaAs, causing the formation of a uniformly reacted layer. That is why in the present metallization scheme a uniform alloying can be expected at the original Ni(50 Å)/GaAs interface. Also, most of the Ge present in the second layer (170 Å) on top of Ni (50 Å) can be expected to diffuse uniformly into the GaAs, since Ge is known to be a fast diffuser in GaAs in the presence of Ni [15]. Au may have diffused to the GaAs surface through the Ni-Ge rich region at the original metal/GaAs interface, and thereby dissociated more GaAs. Since Ge is present close to the original metal/GaAs interface, it is readily available for doping in GaAs by occupying the Ga sites to form a highly doped region.

4.1.2 EDS Analysis

In order to examine the composition of the metal/GaAs interfacial region, EDS analysis was performed by operating the H-600 electron microscope in the STEM mode with an electron probe size of 200 Å. Based on the EDS analysis, the interfacial region can best be described as a distribution of two different compositions. There are Ni rich, Au deficient regions (Au free in most cases) and Au rich, Ni deficient regions. Several X-ray spectra of the interfacial region were taken and it has been found that the alloyed areas having uniform contrast (see Figure 4.3) are mostly Ni rich (Au free) regions. Mostly Au rich regions are found immediately above the original metal/GaAs interface. Typical X-ray spectrum of the Ni and Au rich regions is shown in Figure 4.6. Very distinct Ge $K\alpha$ peaks were observed in the Ni rich regions. Since the Au $L\alpha$ and Ge $K\alpha$ peaks lie very close to each other in the X-ray spectrum, the Ge $k\alpha$ peak could not be resolved in the Au rich regions.



(a)



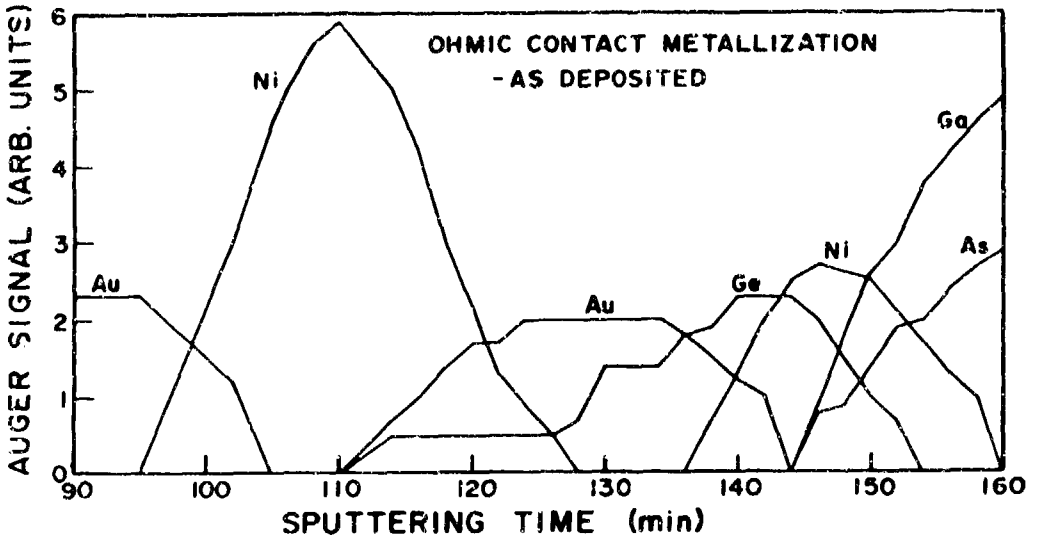
(b)

Figure 4.6 Typical EDS spectra of (a) Ni and (b) Au rich regions.

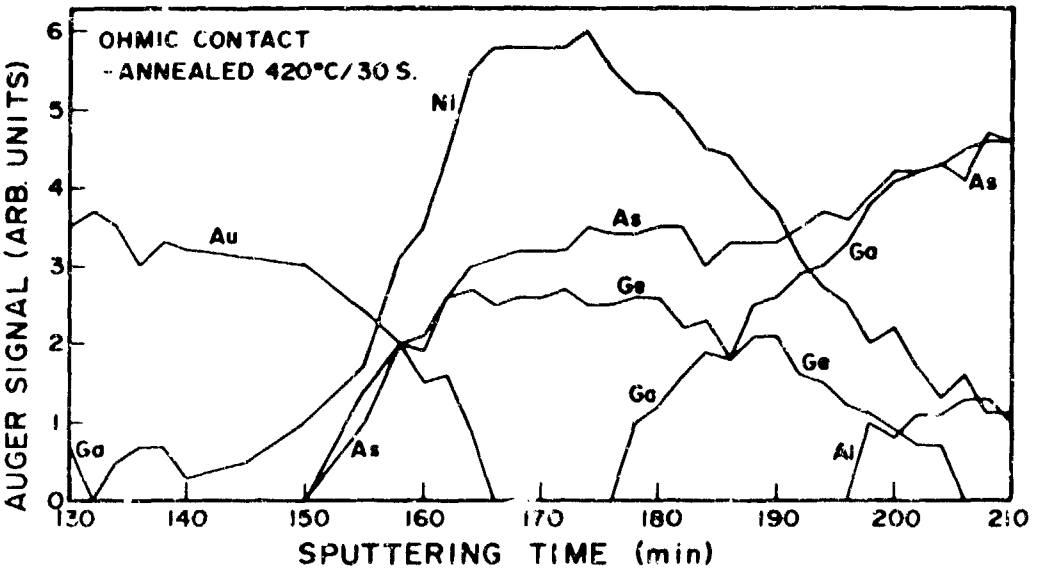
However, the presence of the Ge Kα line in the X-ray spectrum of the Au rich regions was confirmed in the following manner. An X-ray spectrum of the surface of the metallized region (containing mostly Au) was used to obtain the peak height ratio of Au Mα/Au Lα. The peak height ratios were then compared with similar ratios obtained from the EDS spectra of the Au rich regions. The peak height ratio for the Au rich regions was invariably found to be less than that of the pure Au region, indicating the contribution of Ge Kα. The presence of Au, Ni, and Ge was observed in the lateral and deeper alloyed regions at the contact edge.

4.1.3 Auger Analysis

In order to obtain a qualitative view of the distribution of elements in MODFET contacts, Auger analysis was carried out at AFWAL/AADR on metallized wafers both before and after annealing. Depth profiles of the constituent elements were obtained by sputtering in an argon plasma and measuring the corresponding Auger peak signals. The elemental profiles in the vicinity of the metallization/semiconductor interface for both as-deposited and annealed contacts are shown in Figure 4.7. In the case of the as-deposited contact (Figure 4.7a), only an Au signal, corresponding to the top layer, was detected during the first 95 minutes sputtering time after which a Ni signal, corresponding to the next layer, was observed. The sequence of Au, Ge, Ni, Ga/As signals followed according to the order of the as-deposited layers on GaAs. The overlapping of the signals can be attributed partly to mixing effects during the sputtering process and partly to the finite signal extraction depth (~ 50 Å). After annealing at 420°C for 30 second, considerable redistribution of the constituent elements takes place, as shown in Figure 4.7(b). Since the analysis area is a spot with diameter ≈ 1 mm, the depth profiles measured represent an average and do not reveal any microscopic lateral variations. Although only the profiles for the sputtering period 130 to 210 min are shown, considerable outdiffusion of Ga into the surface Au layer was observed with a build up at the surface. The observation of a Ni-Ge-As layer between the Au rich layer and the GaAs substrate is in good agreement with the electron diffraction



(a)



(b)

Figure 4.7 Auger profiles of AlGaAs/GaAs MODFET ohmic contacts (a) as-deposited and (b) after annealing at 420°C for 30 second.

pattern and EDS analyses. The deep Au rich spikes, which were observed from TEM micrographs, were not resolved in the Auger profiles which probably attests to their low surface area compared with the analysis area. In addition, Ni and Ge signals are found to coexist with an Al signal after a 196 min sputter period. This suggests that Ni and Ge have penetrated near or into the AlGaAs layer and that possibly some outdiffusion of Al has taken place.

4.1.4 Thermal Stressing

Figure 4.8 illustrates the time dependent degradation of the resistance of the fabricated ohmic contacts at 250°C and 300°C. At 250°C, there was an initial resistance increase of 0.02 Ω in the first 10 hours followed by a monotonic degradation of 2.3×10^{-4} Ω/hour. At 300°C, the contact resistance increased by 0.035 Ω in the first 2 hours and degraded at 3.4×10^{-3} Ω/hour thereafter. After 40 hours at 300°C, the contacts became electrically unstable, generally exhibiting a gradual downward current drift at a constant applied potential. As shown in Figure 4.9, the material sheet resistivity (initially 297 Ω/□), measured from the transmission line pattern, was found to initially increase at 250°C and then level off with time. However at 300°C, there was a sudden increase in material resistivity followed by a drop. The drop in material sheet resistivity may be attributed to excessive diffusion of contact material which introduced defect related stress in the semiconductor. If the stress resulted in carrier compensation, then the average resistivity of the material in between the metallization would increase as the spacing decreased. This would result in an effective lowering of the material sheet resistivity as measured from the contact resistivity pattern. A simple lateral outdiffusion of contact material would result in a systematic reduction in contact spacing which would not influence the material sheet resistivity. The defect related stress producing carrier compensation is also consistent with the drift observed in the contact resistance measurement. In this case, as traps were progressively filled the resistivity of the material would drop.

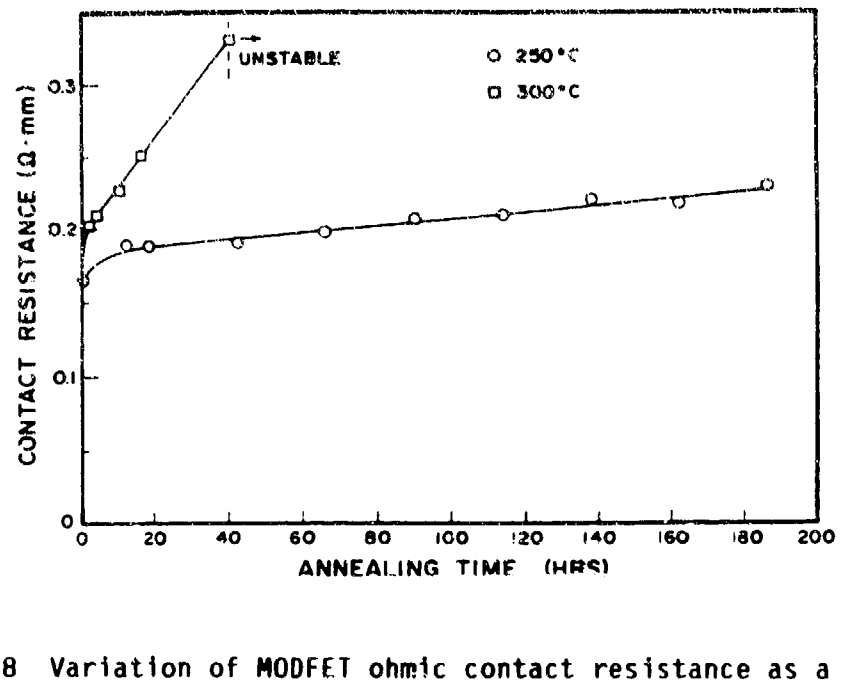


Figure 4.8 Variation of MODFET ohmic contact resistance as a function of anneal time for temperatures of 250°C and 300°C. After 40 hours at 500°C, contacts exhibit current drift at constant applied voltage.

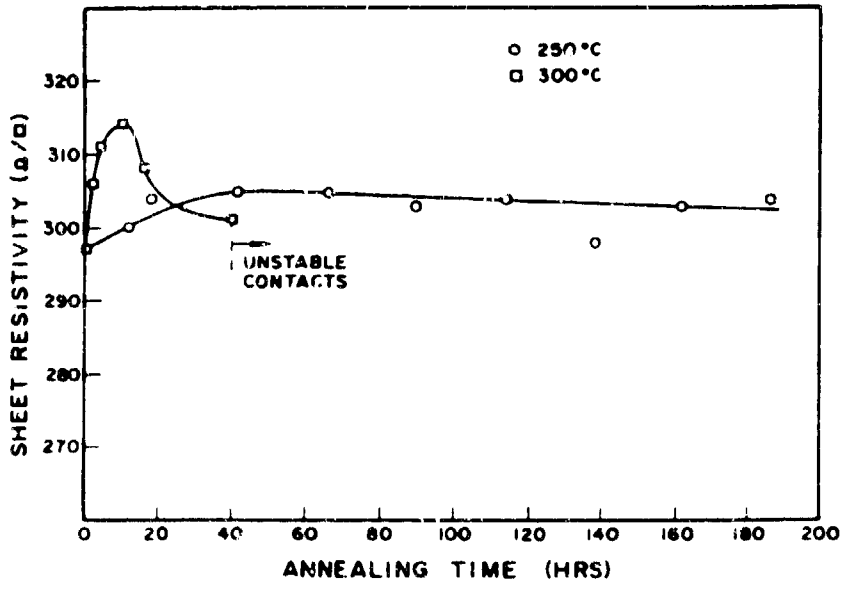


Figure 4.9 Variation of sheet resistivity of MODFET material, determined from TLM contact resistivity pattern, as a function of anneal time.

Cross sectional TEM samples were made of the 300°C/40 hour stressed contacts. Figure 4.10(a) shows a low magnification bright field micrograph of the stressed sample. Frequent penetration of the contact materials in the form of vertical spikes was clearly observed. The penetration in stressed samples was found to be deeper than in the unstressed samples. Figure 4.10(b) shows a high magnification micrograph of one of the spike regions; the penetration depth was found to be 1600 Å. Similar spiking phenomena were also observed at the gap ends. However, no significant difference was observed (between stressed and unstressed structures) in the extent of lateral contact material movement at the edge of the contact gaps. The presence of straight white-line contrast at the original metal/GaAs interface indicates that even after thermal stressing (300°C/40 hour) the intermixing between the contact materials and GaAs takes place via solid state diffusion.

Energy dispersive X-ray analysis was carried out in the regions of deep vertical penetration and in the region of lateral penetration at the edge of contacts. In order to get a qualitative idea of the penetration of the various constituent contact elements, spectra were taken at the positions shown in Figures 4.11 and 4.12. The electron beam spot size used was 200 Å and, therefore, the acquired signal is an average over a volume having a diameter up to ~ 400 Å. The spectra peak heights corresponding to the Au(M_α), Ga(K_α), As(K_α), and Ni(K_α) signals were plotted in Figures 4.11 and 4.12 as a function of position in the vertical and lateral metallization penetrations, respectively. For the vertical penetration, Au maintains a high concentration up to position 3, then drops considerably in the portion of the penetration which extends beyond the mean depth. The Ni concentration is at a maximum near the tip of the visible penetration and drops off in the layer beneath. This suggests that in this localized spike region Ni has considerable mobility and may be driven in by the gold penetration, thus acting as a marker. As would be expected, outdiffusion of both As and Ga is observed. No peak heights were plotted for Al and Ge due to masking in the X-ray spectra by other dominant element peaks.

a

0.15 μm

b

0.063 μm

Figure 4.10 Cross sectional bright-field micrographs of thermally stressed (300°C/40 hour) samples at (a) lower and (b) higher magnification.

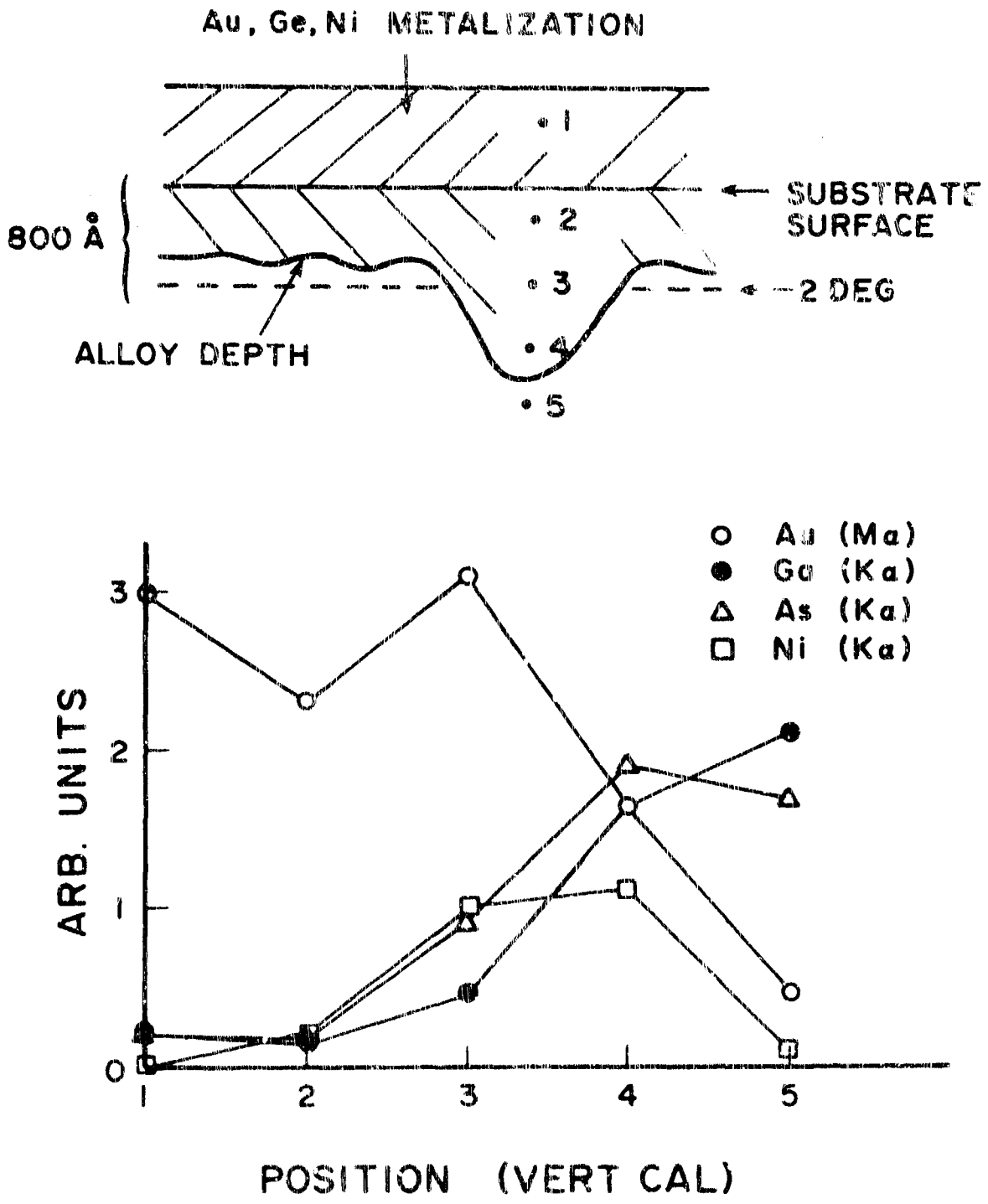


Figure 4.11 Elemental profiles in the central vertical spike zone of a thermally stressed contact as determined from energy dispersive X-ray analysis. The numbers in the schematic cross section denote the analysis positions.

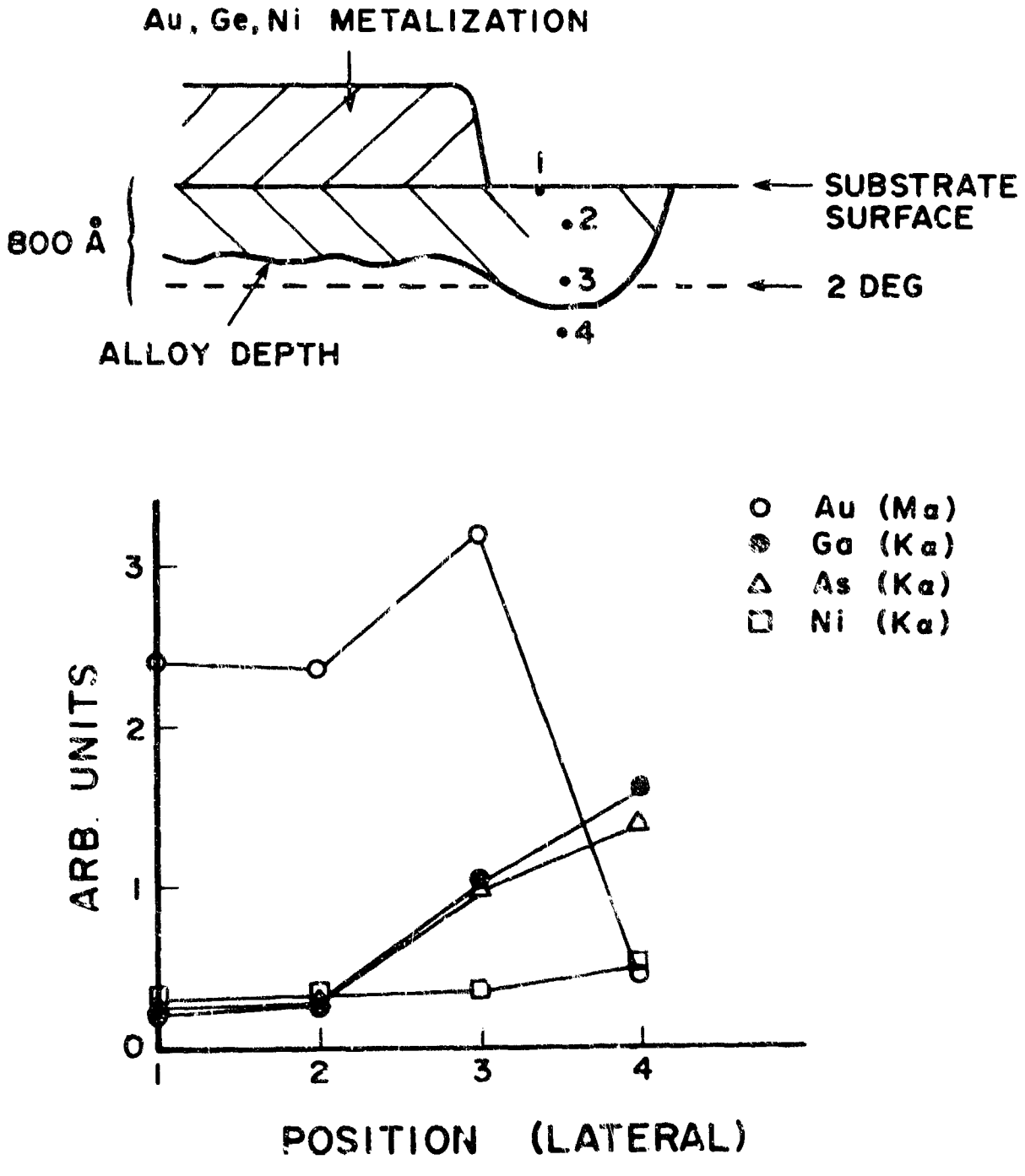


Figure 4.12 Elemental profiles in the laterally penetrated region of a thermally stressed contact as determined from energy dispersive X-ray analysis. The numbers in the schematic cross section denote the analysis positions.

In the case of lateral penetration at the edge of the contact, Ni again appeared to accumulate at the edge of the penetration. The trends for the other detected elements were similar to those for the vertical spike penetration.

4.2 RAPID THERMAL ANNEALING OF MODFET CONTACTS

Rapid Thermal Annealing (RTA) of AlGaAs/GaAs MODFET ohmic contacts had been reported to yield lower contact resistivities than conventional furnace annealing [16-19]. Typically, the contacts were rapidly heated to a peak temperature, considerably greater than in a conventional anneal, and then cooled down after either a very short or zero dwell time. However, no TEM analysis of the depth distribution of the various metallurgical phases and the physical structure of the contacts was reported. Since the possible explanations for the improved electrical behavior were unclear, a study was undertaken to determine the structure and electrical behavior of the contacts in this program.

In these investigations, the metallization and AlGaAs/GaAs MODFET material structure were the same as for the conventionally annealed ohmic contacts. The basic test structure pattern, which included the TLM pattern, was again used for contact resistance measurement and TEM sample preparation. In order to form ohmic contacts, the patterned wafer was transient annealed in a conventional quartz furnace using a flowing N_2 ambient.

With the furnace temperature stabilized at 750°C, the wafer was introduced rapidly into the hot zone. The temperature of a dummy GaAs sample placed next to the wafer was monitored with a thermocouple junction, and at the peak temperature the wafer was quickly withdrawn from the furnace. The temperature cycle for a transient anneal to a peak temperature of 525°C is shown in Figure 4.13. The rise time to the peak temperature was 50 second. We found this anneal cycle to produce ohmic contacts which had a uniform surface morphology and a contact resistivity of typically ~ 0.1 Ωmm. For peak anneal temperatures greater than 525°C, the contact morphology began to deteriorate while for

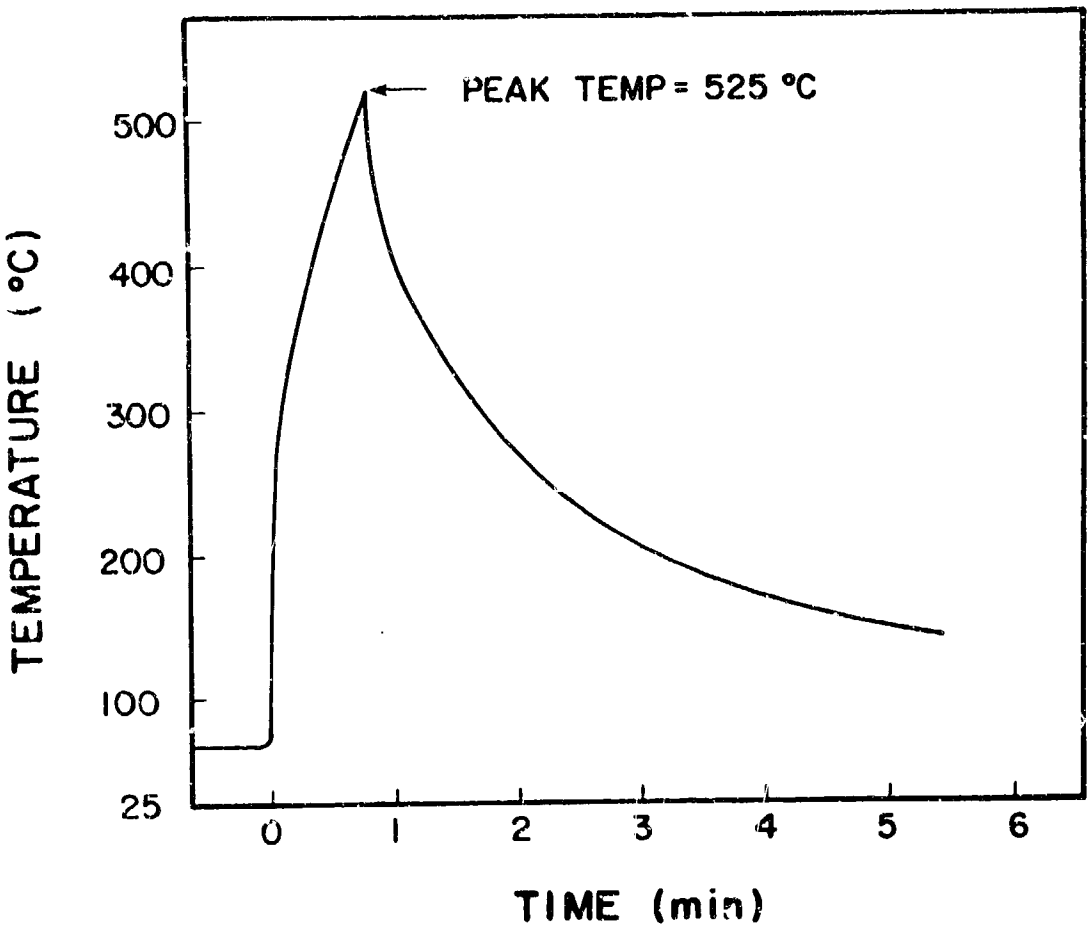
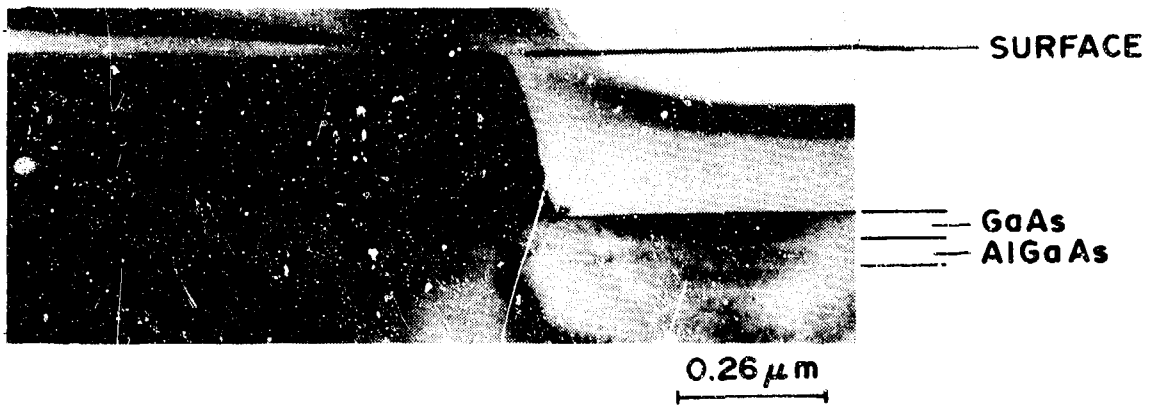


Figure 4.13 Rapid thermal anneal cycle of MODFET ohmic contact.

temperatures less than 525°C the contact resistivity increased. A corresponding optimized conventional anneal at 420°C for 30 seconds yielded a contact resistivity of 0.24 Ωmm for the same metallization and material. These results indicate that significant reductions in contact resistivity to MODFET material may be attained if a transient anneal cycle of the type used in these investigations is employed.

Figure 4.14(a) shows the cross sectional bright field micrograph, at one of the metallization edges of an as-deposited contact. Although no movement of the metallization parallel to the GaAs surface is observed, some reaction at the metal pad-GaAs interface occurs. This is not surprising since Ni is known to react with GaAs during deposition [20]. Figure 4.14(b) shows the cross sectional bright field micrograph of one of the metallization edges of the sample annealed to a peak



(a)

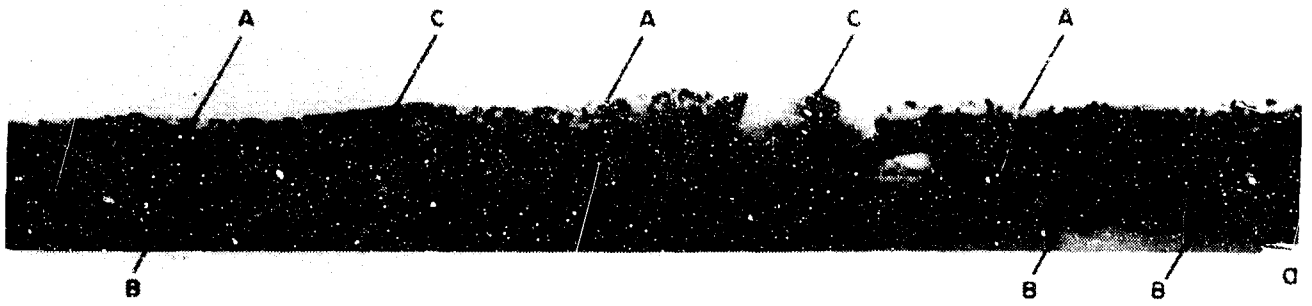
(b)

Figure 4.14 Cross sectional bright-field micrographs of the metallization edges of the (a) as-deposited and (b) annealed (525°C, 0 second) samples.

temperature of 525°C. Movement of the metallization both parallel and perpendicular (830 Å) to the GaAs surface has occurred. After annealing, the metallization edge is no longer straight as observed in the as-deposited and conventionally alloyed samples. It seems that some kind of sliding (flow) of the metallization has occurred. The observed structure of the metallization edges has significant implications for submicron device structure design, since it places a limit on the minimum geometries employed if device reliability is to be maintained.

Figure 4.15(a) represents a typical cross sectional bright field micrograph of the region underneath one of the contact pads. Figure 4.15(b) shows the corresponding selected area diffraction pattern. The diffraction pattern was recorded after orienting the GaAs along the [110] zone axis. Figure 4.15(c) represents the dark field micrograph obtained by putting the objective aperture at one of the diffraction spots having d-spacings equal to ~ 2.35 Å (note that this d-spacing corresponds to the 111 reflection of Au). This particular diffraction spot is marked by an arrow in Figure 4.15(b). The dark field micrograph clearly delineates the Au rich region as a layered structure. Also, we were able to orient the Au rich region only in the [110] zone axis orientation and the lattice parameter obtained was very close to that of pure Au.

Three different regions are clearly evident from Figure 4.15(a). Region A, which is the top layer, region B which is the alloyed layer with GaAs and region C which is found embedded in region A and lying above the alloyed layer. The top portion of the metallization in this particular region of the sample was sputtered away during ion milling. EDS analysis was performed to determine the composition of these three regions. Figures 4.16(a,b,c) show the EDS spectra of the regions A, B, and C, respectively. In this case, the EDS analysis was carried out on a Philips 400 electron microscope equipped with a field emission gun. The probe size was about 50 Å and the spectra were collected for 2 min. In accordance with the structural analysis, described above, region A was found to be Au rich. The alloyed layer (region B) consisted of Ni-As(Ge) while Ni-Ge rich phase was observed in region C. The Au rich region was most often found to be lying above the alloyed (NiAsGe) region.



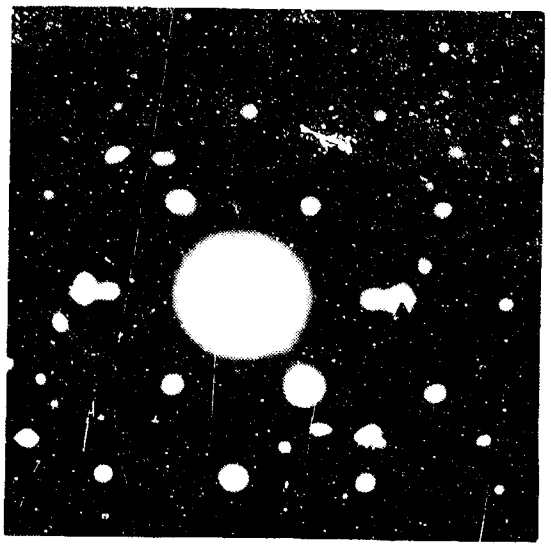


Figure 4.15 (a) Cross sectional bright-field micrograph of the region underneath one of the contact pads. (b) Selected area diffraction pattern, corresponding to (a).
(c) Cross sectional dark-field micrograph of the region shown in (a).

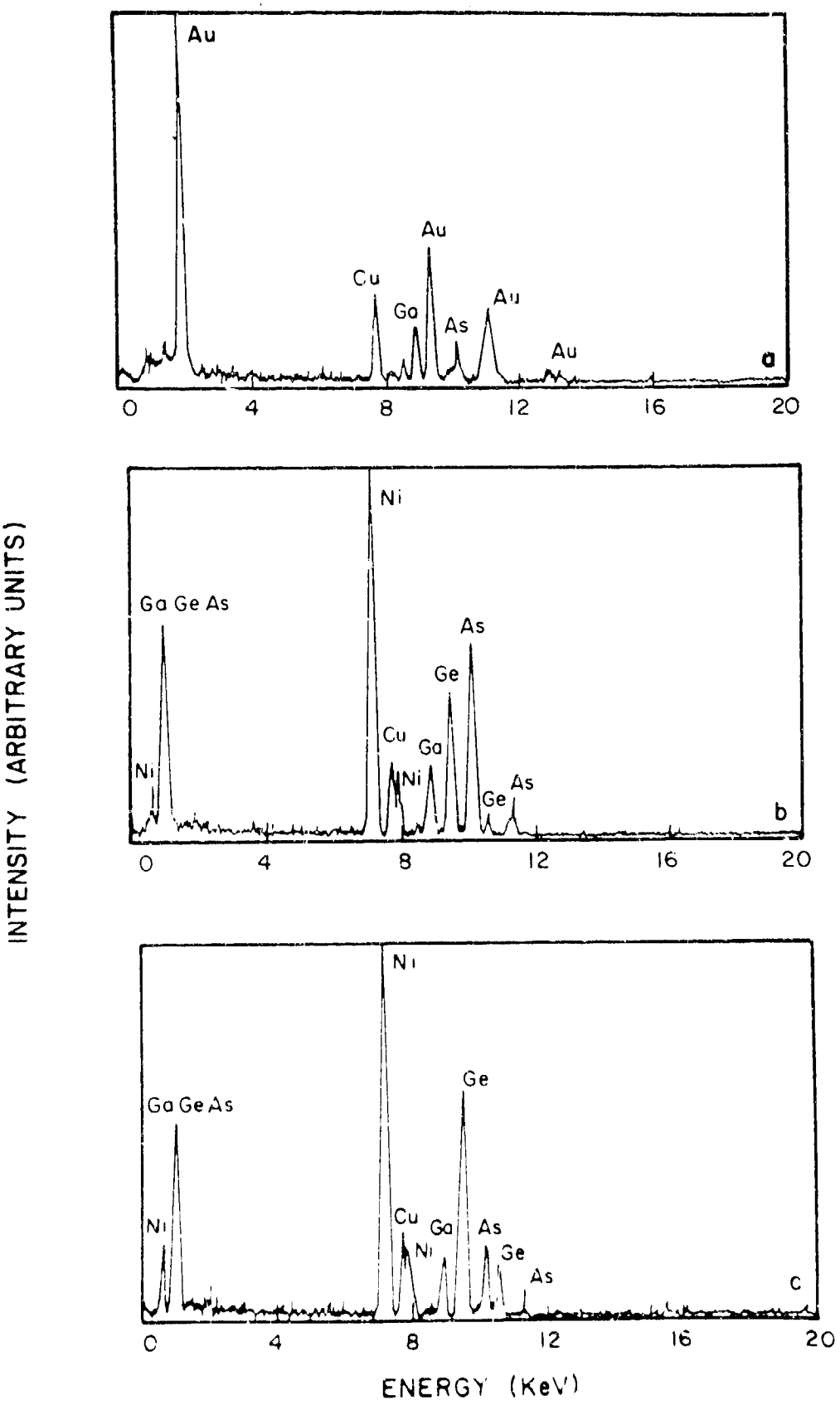


Figure 4.16 Typical EDS spectra of the regions A(a), B(b), and C(c) marked in Figure 4.15 (a).

However, at one point, the Au rich region had protruded through the alloyed region and contacted the GaAs directly. Figure 4.17 represents a high resolution image of the area. The interface between the Au rich phase and GaAs is marked by arrows. The Ni-As(Ge) rich phase (region B) are also marked in Figure 4.17. EDS analysis also indicated more outward diffusion of Ga than As.

From the TEM cross sections of the contact edges, it appears that the contact metallization only penetrates as far as the AlGaAs and does not reach the AlGaAs/GaAs buffer layer interface. Consequently, in this region, contact would only be made directly to the n^+ GaAs and n^+ AlGaAs layers. This implies that the 2DEG current component of the MODFET source-drain current would then be required to pass through the AlGaAs layer. In contrast, the conventionally annealed contacts, the edge metallization was found to penetrate all the way through to the GaAs buffer layer, thus suggesting that direct contact to the 2DEG was possible. The reduction in contact resistance obtained by RTA compared with conventional annealing suggests that deep penetration is not essential for obtaining low contact resistances and that shallower penetration may in fact be preferable. These observations clearly demonstrate the dependence of contact resistance on the physical structure of the contact as well as the composition of the alloy phases.

Figure 4.17 Cross sectional high-resolution image of the area where Au rich phase contacted the GaAs directly.

SECTION V
BIPOLAR INVERSION CHANNEL FIELD EFFECT TRANSISTOR

5.1 INTRODUCTION

Solid-State devices have long been dominated by bipolar junction and field effect types of devices. Bipolar Junction Transistors (BJTs) are recognized for their high frequency, high speed, and high current gain performance; they are used as current modulation devices. Field Effect Transistors (FETs) are recognized for their high transconductance, low power consumption, and integration capability; they are used as voltage modulation devices.

With the continuous progress in processing technology development, devices are made with ever shrinking dimensions. Although by reducing dimensions, devices gain advantages in speed and integration capability, they also encounter problems. For example, in silicon Metal Oxide Semiconductor Field Effect Transistors (Si-MOSFETs), source and drain punch-through and hot-electron injection into the gate dioxide result in a reliability problem, especially when gate lengths are reduced below a certain limit. In BJTs, emitter and collector punch-through and high-base resistance result in null function or inferior performance when base dimensions are reduced.

With the advent of Molecular Beam Epitaxy (MBE) and Metalorganic Chemical Vapor Deposition (MOCVD) crystal growth technologies, a number of III-V compound semiconductor heterostructure device concepts, developed either recently or a number of years ago, have been demonstrated. Among these is the Heterojunction Bipolar Transistor (HBT) which, as originally conceived, is essentially a Bipolar Transistor (BT) with a wide band gap emitter. Although a wide range of material choices exist for fabricating this device, the most extensively studied combination is AlGaAs/GaAs. For an n-p-n HBT, the basic structure consists of an n-doped AlGaAs emitter, a heavily p-doped GaAs base and an n-doped GaAs collector. Because of the band gap discontinuity between the emitter and base, the emitter injection efficiency is very high and this, in turn, results in high gain. The band discontinuity, which limits

the hole component of the emitter current also allows the use of higher doping in the base compared with a BJT. The freedom to dope the base highly also enables the base width to be reduced without having to pay the penalty of a high base resistance which consequently improves the high frequency performance of the HBT.

Although the advanced devices made possible by today's technology have shown impressive performances, a search for even higher performance devices capable of meeting future advanced microwave and digital system requirements continues. The need for devices with high gain-bandwidth products, which present day devices may not be able to attain, necessitates a reexamination of design concepts, new material possibilities or a combination of both. The Bipolar Inversion Channel Field Effect Transistor (BICFET) is a device which has the potential to meet the requirements of future high performance devices [21]. Specifically, the potential advantages of the BICFET are

1. High current density and current gain, equal to or better than for an HBT.
2. Higher maximum operating frequency and switching performance than state-of-the-art bipolar and MOS transistors.
3. No punch-through effects.
4. High circuit integration capability.
5. Freedom from the scaling limitations of existing devices.
6. Low input capacitance.

5.2 SEMI-ANALYTICAL THEORY OF THE BICFET

5.2.1 Structure of the Bipolar Inversion Channel Field Effect Transistor

The physical structure and corresponding band diagrams of a proposed n-channel BICFET are shown in Figures. 5.1 and 5.2, respectively. The BICFET structure is similar to that of a p-n-p HBT except that the base is replaced by a heavily doped n-type spike layer. The role of the spike layer is solely to provide sheet charge which produces band bending such that when a bias is applied to the device structure a strong inversion channel composed of electrons is formed in

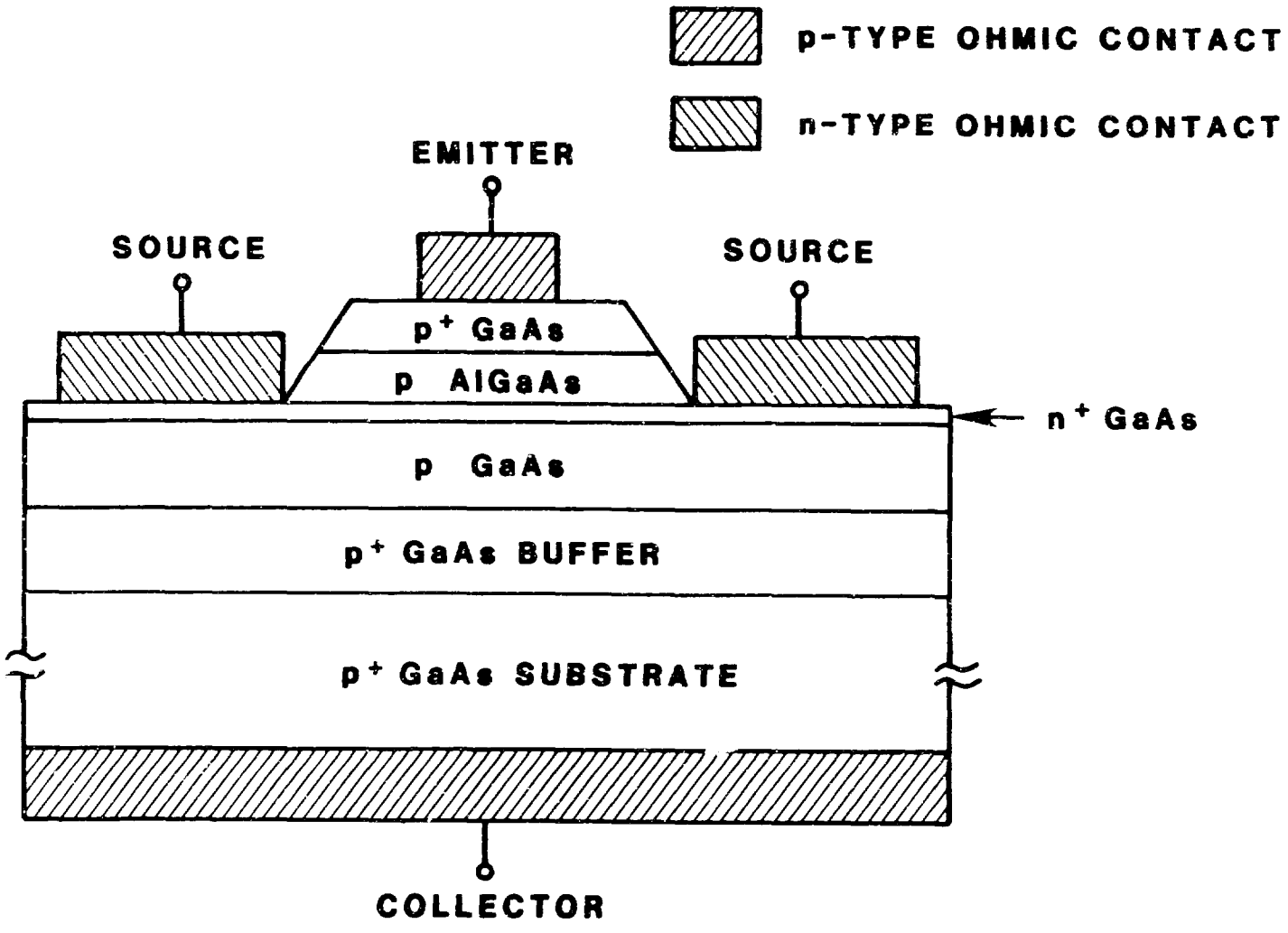


Figure 5.1 Schematic cross section of n-channel BICFET.

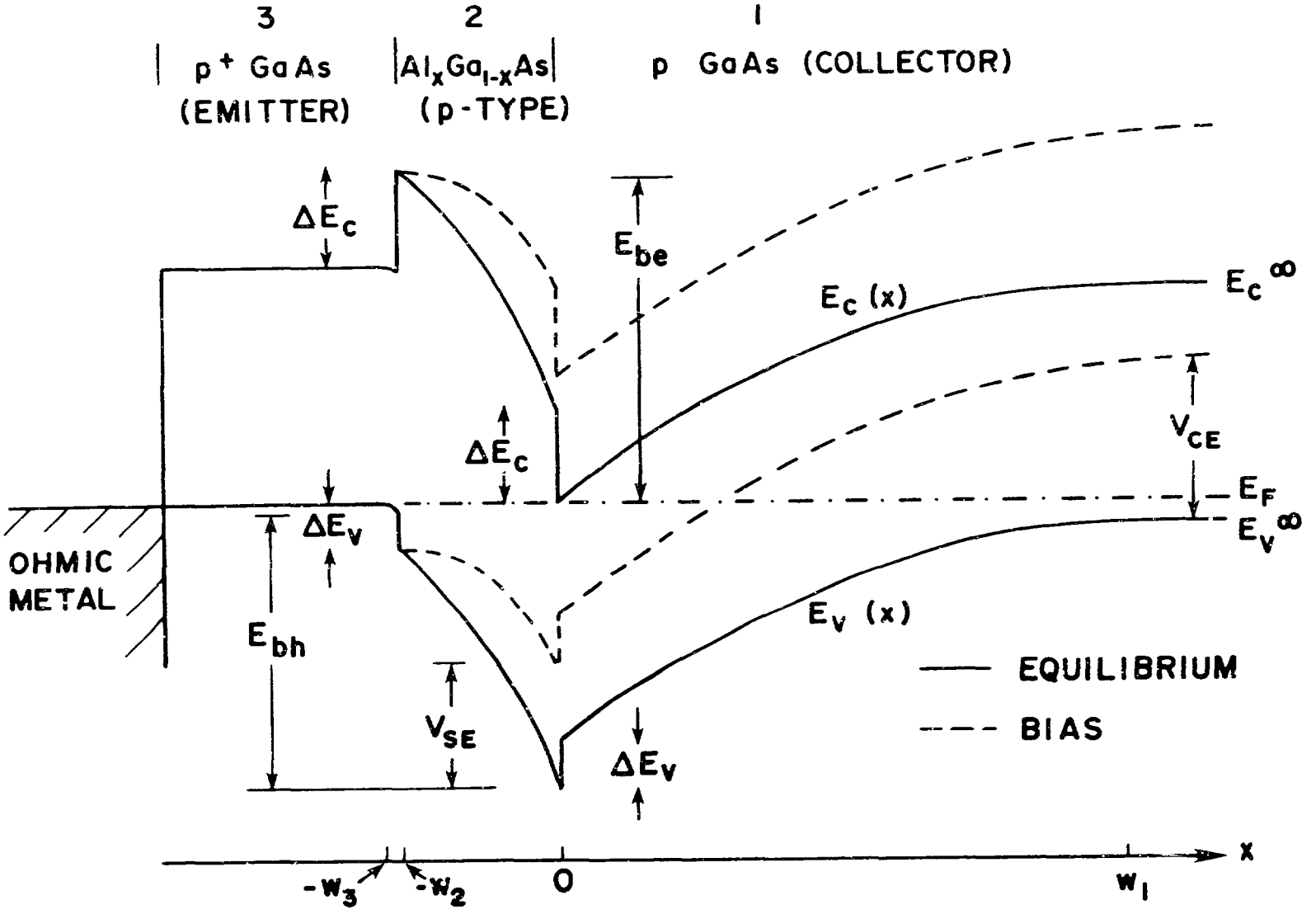


Figure 5.2 Schematic band structure of n-channel BICFET.

the semiconductor layer (collector) adjacent to the wide band gap layer. Because of the similarity with an MOS channel, this inversion layer is designated as the source. When the BICFET is biased in a transistor mode of operation, the source current effectively modulates the majority carrier current injected from the emitter. In this sense, the source in the BICFET is equivalent to the base in a bipolar transistor.

In a conventional HBT/BJT, parameters of the base such as width and doping concentration play a very important role in device performance. Non-optimized parameters can cause base punch-through, base narrowing, base crowding, base push-out during high current injection, etc. In a BICFET, since there is no base physically to operate, some of those base-related problems such as punch-through and narrowing do not exist. In addition, since the BICFET does not have a base layer, it does not have the associated large diffusion capacitance found in conventional HBTs and BJTs. Moreover, the transport time through the inversion channel is almost negligible. This enables the BICFET to operate at high speed and high frequency. There is a wide range of material combinations that is suitable for BICFET fabrication. Since the material combination $Al_xGa_{1-x}As$ lattice matched to GaAs has been extensively studied and can be grown with high quality interfaces, it will be adopted in these discussions.

In the following, the characteristics of each part of the BICFET shown in Figure 5.1 will be described.

1. Emitter contact layer: A heavily p-type doped GaAs layer which is capable of injecting a large number of carriers into the device and which also serves as a contacting layer for an external emitter ohmic contact. In their original paper, Taylor and Simmons [21] proposed a metal with a small work function difference compared to AlGaAs. However, due to the existence of AlGaAs surface states, the metal/semiconductor barrier height would not, in general, be determined by the difference in work functions but rather by Fermi level pinning at the surface of the semiconductor [22-24]. Since the Fermi level is pinned mid band, the metal/semiconductor barrier height is too high for BICFET applications.

2. Semi-insulator (SI) layer: A semiconductor layer with a band gap larger than that of the adjacent semiconductor collector layer. Due to the doping in this layer, it is not really semi-insulating by nature; however, due to the wide band gap and in keeping with the original terminology, it will be referred to as such. The transport mechanism for both electrons and holes across the SI layer is assumed to be thermionic emission-diffusion limited. The holes injected from the emitter see an immediate barrier height of magnitude ΔE_v determined by the valence band discontinuity and the electrons injected from the source channel see an immediate barrier height of magnitude ΔE_c determined by the conduction band discontinuity. For the $Al_{0.3}Ga_{0.7}As/GaAs$ heterojunction, the ratio of the conduction and valence band discontinuities is taken as 65/35 which gives ΔE_c = 0.243 eV and ΔE_v = 0.131 eV [12]. Besides the suitable discontinuities in the conduction and valence bands at the heterojunction, there are several other requirements for the SI layer. First, it is doped with the same type of dopant as in the emitter, p-type in this case. Second, it must be completely depleted at thermal equilibrium and during BICFET operation [21]. Therefore, the dopant concentration in the SI layer cannot be too high or the thickness of the SI layer cannot be too large. The dopant concentration in the SI layer cannot be too low either, or space-charge-limited conduction will turn on too soon (space-charge-limited current is proportional to the square of the applied forward voltage, which is inferior to the thermionic emission current which is exponentially proportional to applied forward voltage) [25].

3. Spike layer: This layer is heavily doped n-type GaAs. Ideally, it is composed of only several atomic layers. At thermal equilibrium, this layer is assumed to be totally depleted. The immobile charge left in this layer is sufficiently great to deplete the entire SI region and parts of the emitter and collector layers. During active BICFET operation, an inversion channel is formed in the vicinity of the spike layer. In the BICFET I-V calculation described later, the spike layer is treated as a sheet of charge with no existing thickness. The spike layer is placed in the GaAs rather than AlGaAs for two main

reasons. First, for AlAs mole fractions greater than 0.2 in AlGaAs, a significant number of electron traps are detected which are attributed to donor-related complexes (DX centers). These traps may be detrimental to BICFET operation at low temperature. Second, for silicon doping by MBE, it appears that the maximum attainable donor concentration is lower in AlGaAs than in GaAs. This effect may be partly due to a larger fraction of the Si atoms being incorporated as acceptors due to the amphoteric nature of Si [26].

4. Collector: This layer is p-type doped GaAs. The dopant concentration in this layer should not be too low, otherwise the current capability will suffer due to a low space-charge-limited current. Also, the high frequency performance will suffer due to a long transit time through the collector depletion region. The dopant concentration should not be too high either, since it will not yield a saturated I-V behavior in common-emitter mode (the unsaturated I-V curve causes a lower inverter pull-down power, a lower noise margin, an intrinsic impedance which dominates load impedance, etc.). The thickness of this layer should be able to accommodate the depletion width for the applied bias range.

5.2.2 Assumptions

In this semi-analytical model, the band diagrams for both thermal equilibrium and bias cases and the I-V characteristics of the BICFET are derived based on the following assumptions:

1. Maxwell-Boltzmann statistics are applicable to calculate the charge carrier concentration.

2. The SI layer is completely depleted under the whole range of operating voltages.

3. The carrier transport in the SI layer is thermionic emission-diffusion limited. The tunneling current is not included in the calculation.

4. The charge in the spike layer is determined with a negligible Fermi-factor. The thickness of the spike layer is assumed negligible.

5. Carrier recombination in the SI layer, depletion regions of the emitter and collector and interface states at the heterojunction, is negligible.

5.2.3 Equilibrium Case

In this section, the one-dimensional band diagram calculation for the structure shown in Figure 5.1 is outlined. Figure 5.2 shows a schematic band diagram of the structure at thermal equilibrium. The band structure is separated into three regions. In region 1, where $0 < x < \omega_1$, ω_1 is the position in the collector where band bending stops. In region 2, where $-\omega_2 < x < 0$, ω_2 is the thickness of the SI layer. In region 3, where $-\omega_3 < x < -\omega_2$, $-\omega_3$ is the position in the emitter where band bending starts. $E_c(x)$ and $E_v(x)$ are the conduction and valence band energies as a function of position, respectively. For this structure, Poisson's equation is given by

$$\frac{d^2E_c(x)}{dx^2} = \frac{q^2}{\varepsilon(x)} [N_D(x) - N_A(x) + p(x) - n(x)] \tag{5.1}$$

and

$$E_v(x) = E_c(x) - E_g(x) \tag{5.2}$$

where $E_g(x)$ is the band gap as a function of position; $\varepsilon(x)$ is the dielectric constant as a function of x; $N_D(x)$ and $N_A(x)$ are the immobile charge concentrations of donors and acceptors as functions of x, respectively; n(x) and p(x) are the electron and hole concentrations as functions of x, respectively; and q is the unit electronic charge. $E_c(x)$ is also given by

$$E_c(x) = -q\phi(x) \tag{5.3}$$

where $\phi(x)$ is the electric potential as a function of x. For region 1, solution of Eq. (5.1) gives the electric field at x = 0 (designated $x = 0^+$) as

$$\underline{E}(0^+) = \sqrt{\frac{2}{\epsilon_s}} \left[N_{A1}(E_C^{\infty} - E_S) - kT(n(\omega_1) + n(0^+) - P(0^+) - P(\omega_1) \right]^{1/2} \tag{5.4}$$

where

$$\underline{E}(0^+) = -q \frac{d\phi}{dx}(0^+) , \tag{5.5}$$

E_s is the conduction band energy at $x = 0^+$ and ϵ_s is the dielectric constant of the collector layer.

For region 2, assuming total depletion, derivation of the conduction band energy gives

$$E_C(x) = \frac{q^2}{\epsilon_{SI}} (-N_{A2}) \frac{x^2}{2} + q\underline{E}(0^-)x + (E_S + \Delta E_C) \tag{5.6}$$

where ϵ_{SI} is the dielectric constant of the AlGaAs and $\underline{E}(0^-)$ is the electric field at x = 0 for the AlGaAs side. The electric fields $\underline{E}(0^+)$ and $\underline{E}(0^-)$ are related by

$$\epsilon_{SI}\underline{E}(0^-) = -[Q_i - \epsilon_s\underline{E}(0^+)] \tag{5.7}$$

where Q_i is the spike layer charge.

For region 3, the electric field at $x = -w_2$ is given by

$$\underline{E}(-w_2^-) = -\sqrt{\frac{2}{\varepsilon_s}}\left\{-N_{A3}[E_c(-w_2^-) - E_c(-w_3)] + kT\left[P(-w_2^-) - P(-w_3) + n(-w_2^-) - n(-w_3)\right]\right\}^{1/2} \quad (5.8)$$

where

$$\varepsilon_s \underline{E}(-w_2^-) = \varepsilon_{SI}\underline{E}(-w_2^+) \quad (5.9)$$

Eqs. (5.4) through (5.9) form a series of simultaneous equations which together with the equations $E_c(0^+) + \Delta E_c = E_c(0^-)$ and $E_c(-w_2^+) = E_c(-w_2^-) + \Delta E_c$ can be solved iteratively to give $E_c(0^+)$, $\underline{E}_c(0^+)$, $E_c(0^-)$, $\underline{E}_c(0^-)$, $E_c(-w_2^+)$, $\underline{E}_c(-w_2^+)$, $E_c(-w_2^-)$, and $\underline{E}_c(-w_2^-)$. These discrete points in the conduction band allow the construction of the band diagram. Figure 5.3 shows the band structure for a wide band gap layer thickness of 350 Å where the Fermi energy of the system is set to zero.

5.2.4 Bias Case

In their original paper, Taylor and Simmons [21] used a thermionic emission-diffusion approach to calculate the I-V behavior of a BICFET. Their analytical formulations were adopted to calculate the band diagram under bias. The calculation of the band diagram under bias is very similar to that derived for the thermal equilibrium case, therefore, only the key equations are described here. The source current density J_s is given by

$$J_s = qV_{ni}n_o e^{-(E_{be}/kT)} + \frac{qD_n}{L_n}\left[n_o e^{(-E_c^{\infty}+E_s)/kT} - n_{po}\right] \quad (5.10)$$

where the first term on the right is the electron current flowing through the SI layer, and the second term is the diffusion current from the source to collector. E_{be} is the energy barrier that the electrons have to overcome before they reach the emitter. V_{ni} is the effective drift

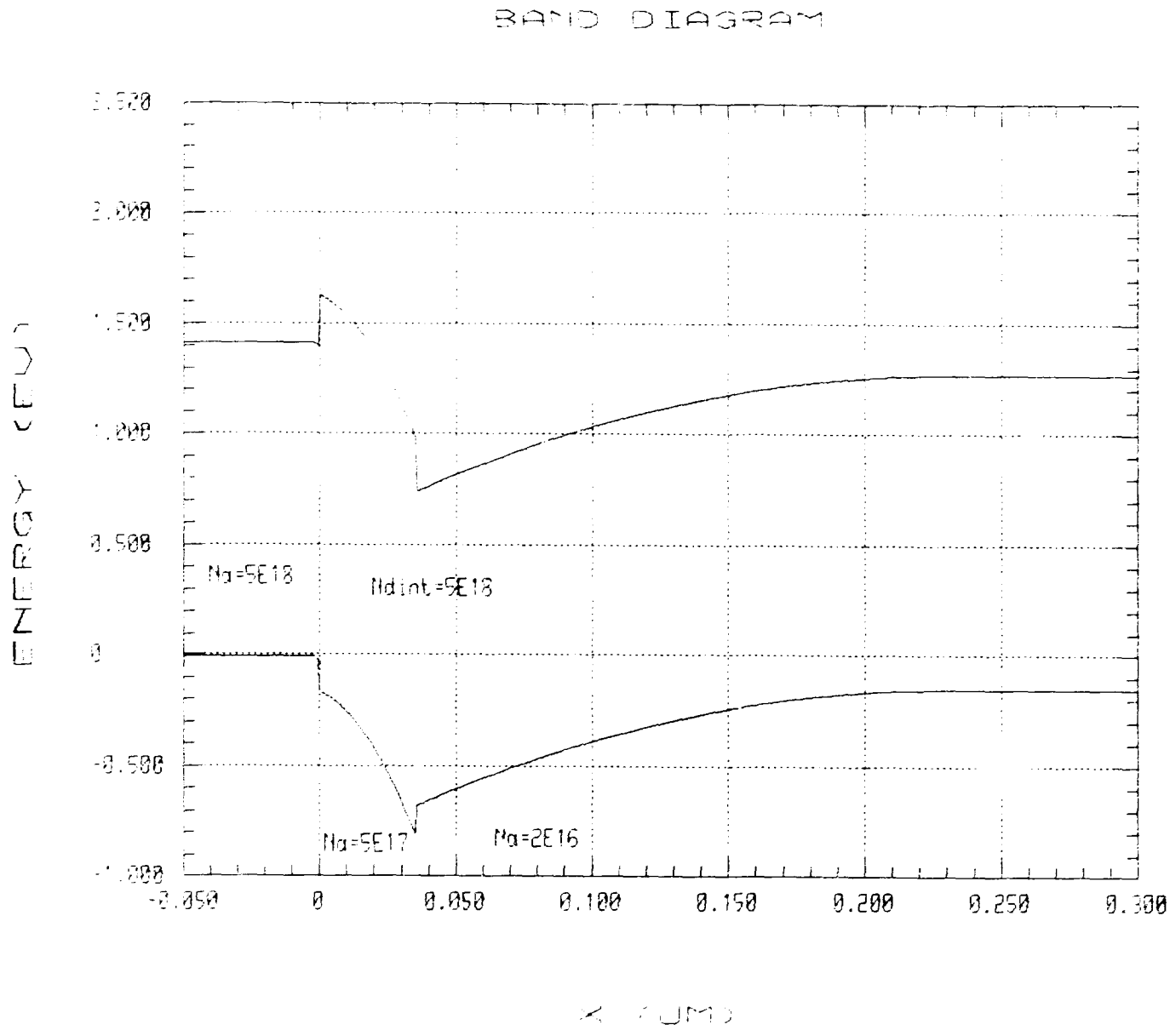


Figure 5.3 Calculated band structure of a BICFET with a 350Å AlGaAs layer.

velocity of electrons flowing through the SI layer, and D_n and L_n are the diffusion coefficient and length, respectively, of electrons in the collector. n_o is the electron concentration at the heterojunction between the SI and collector. n_{po} is the thermal-equilibrium electron concentration in the collector. The collector current is given by

$$J_c = qV_{pi}N_v e^{-(E_{bh}/kT)} - \frac{qD_n}{L_n}\left[n_o e^{(-E_c^{\infty}+E_s)/kT} - n_{po}\right] \tag{5.11}$$

where the first term on the right is the hole current flowing through the SI layer, and the second term on the right is the same as in Eq. (5.10). E_{bh} is the energy barrier that the holes have to overcome before they reach the source/collector. V_{pi} is the effective velocity of holes flowing through the SI layer. The current contribution of the second term in both Eqs. (5.10) and (5.11), as will be discussed, is very small when $|V_{ce}| > 0.4$ volts. From Eqs. (5.10) and (5.11), the current gain can then be estimated as

$$G = dJ_c/dJ_s = \frac{V_{pi}N_v}{V_{ni}n_o} e^{(E_{be}-E_{bh})/kT} \tag{5.12}$$

Therefore, high current gain is realized if a large barrier difference exists between majority and minority carriers as they flow through the SI layer.

In region 1, where $0 < x < \omega_1$, Poisson's equation for $E_c(x)$ is

$$\frac{d^2E_c(x)}{dx^2} = \frac{q^2}{\epsilon_s}\left[-N_{A1} - n(x) + \frac{J_c}{qV_{pc}}\right] \tag{5.13}$$

where $J_c = q(V_{pc})(p)$. The electric field at 0^+ is then given by

$$\underline{E}(0^+) = \sqrt{\frac{2}{\varepsilon_s}}\left[\left(N_{A1} - \frac{J}{qV_p}\right)(E_c^{\infty} - E_s) + kTn_o\right]^{1/2} \tag{5.14}$$

Here, n_o is given by

$$n_o = N_c \exp[-(E_s - E_{fo})/kT] \tag{5.15}$$

where E_{fo} is the quasi-Fermi level at 0^+.

In region 2, the expression for $E_c(x)$ becomes

$$E_c(x) = \left[\frac{q^2}{\varepsilon_{SI}} - N_{A2} + \frac{J}{qV_{pi}}\right]\frac{x^2}{2} + q\underline{E}(0^-)x + (E_s + \Delta E_c) \tag{5.16}$$

where the relation between electric field at 0^- and electric field at 0^+ is given by Eq. (5.7).

In region 3, neglecting the contribution of n, the electric field at $x = -\omega_2$ becomes

$$\underline{E}(-w_2^-) = \mp\sqrt{\frac{2}{\varepsilon_s}}\left\{\pm\left[-N_{A3} + \frac{J}{qV_{pc}}\right]\left[E_c(-w_2^+) - \Delta E_c - E_c^{\infty}\right]\right\}^{1/2} \tag{5.17}$$

where the lower sign is used if $\underline{E}(-w_2^+)$ is positive.

As in the case of the equilibrium situation, the series of simultaneous Eqs. (5.10), (5.11), and (5.14) through (5.17) can be solved iteratively to obtain the band structure. The results of the band calculation are shown in Figures 5.4 and 5.5 for wide band gap layer thicknesses of 200 and 350 Å with applied collector-emitter bias. In these two figures, the band bending in both the emitter and collector are

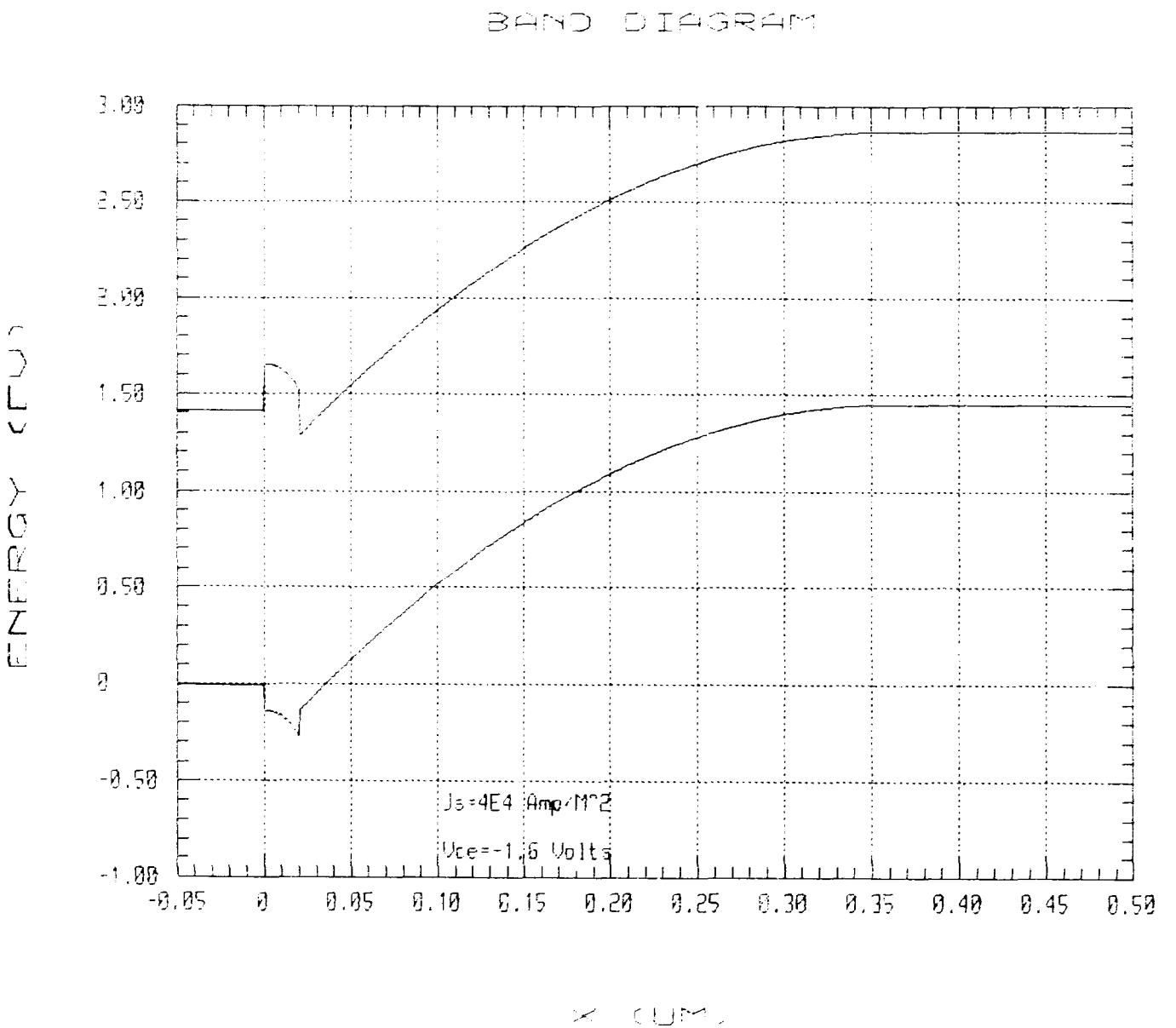


Figure 5.4 Calculated band structure of BICFET with a 200Å AlGaAs layer under bias conditions of $V_{ce} = -1.6V$ and $J_S = 4 \times 10^4$ A/m^2

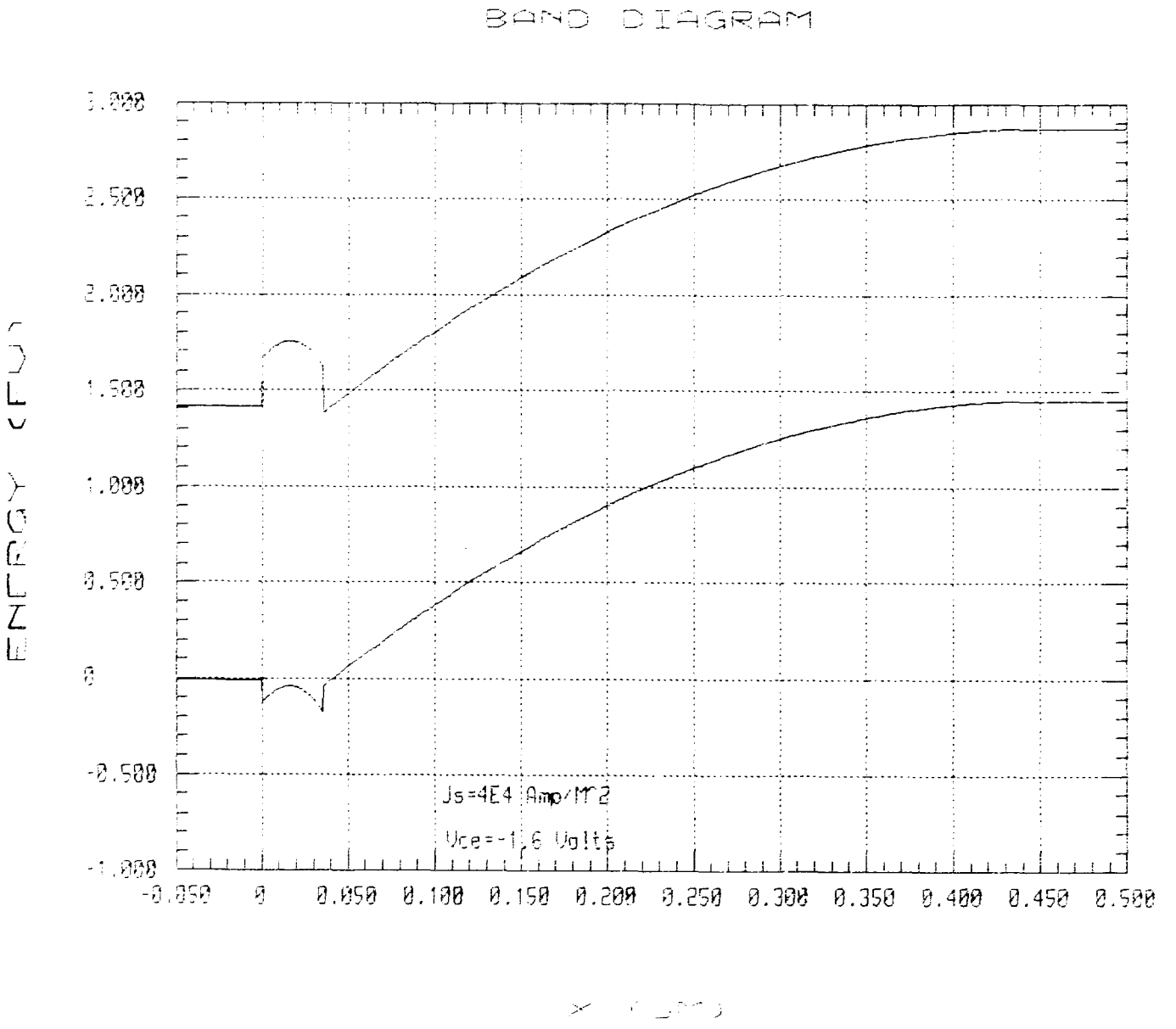


Figure 5.5 Calculated band structure of a BICFET with a 350Å AlGaAs layer under bias conditions of V_{ce} = -1.6V and J_S = 4×10^4 A/m^2

assumed to be due solely to immobile charge. The calculated current-voltage characteristics are shown in Figures 5.6 through 5.8. These results are discussed in the following section.

5.2.5 Results and Discussion

The results of the band diagram calculation and J_c versus V_{ce} are shown in Figures 5.3 through 5.8. In these figures, the default parameters are

N_A in emitter	5×10^{18} cm^{-3}
N_A in SI layer	5×10^{17} cm^{-3}
SI material	$Al_xGa_{1-x}As$, x = 0.3
Thickness of SI layer	350 Å
Conduction band discontinuity	0.243 eV at x = 0.3
Valence band discontinuity	0.131 eV at x = 0.3
N_{int} of spike layer	n type, 2.5×10^{12} cm^{-2}
N_A in collector	2×10^{16} cm^{-3}
Thickness of collector	>0.3 μm
E_g in GaAs	1.43 eV, at Temperature = 300 K
Temperature	300 K

The results of the thermal equilibrium band diagram calculation for a wide band gap layer thickness of 350 Å is shown in Figure 5.3. The 350 Å AlGaAs layer is completely depleted with a depletion layer extension into the highly doped emitter layer. For a 420 Å AlGaAs layer, however, a flat band condition occurs at the emitter layer interface with no depletion layer extension.

Figures 5.4 and 5.5 show the band diagrams for 200 and 350 Å AlGaAs layers with applied bias. In both cases, the applied source current J_s is 4 A cm^{-2} and V_{ce} = -1.6 V. In the case of the

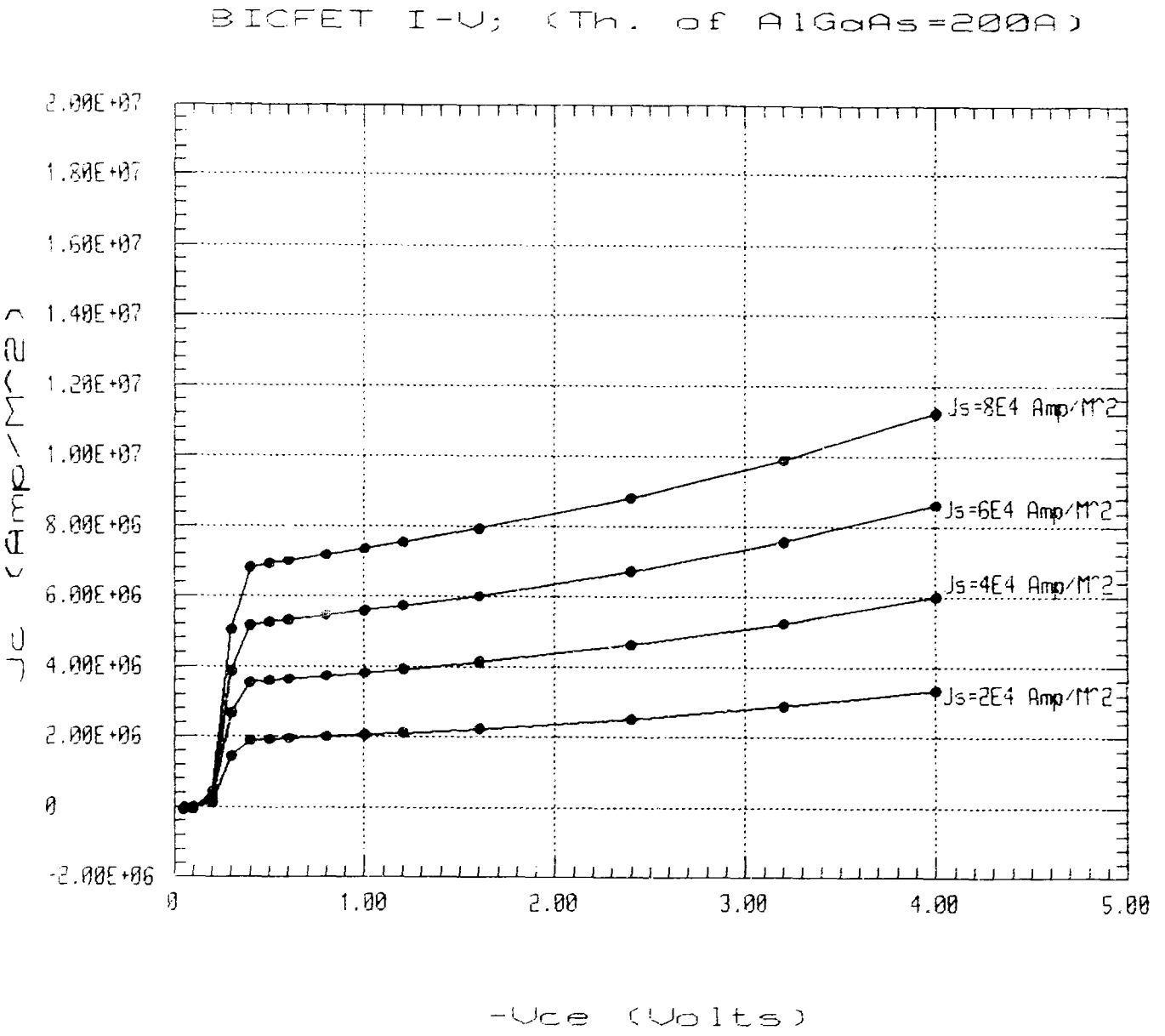


Figure 5.6 Collector current-voltage characteristics for a BICFET with a 200Å AlGaAs layer

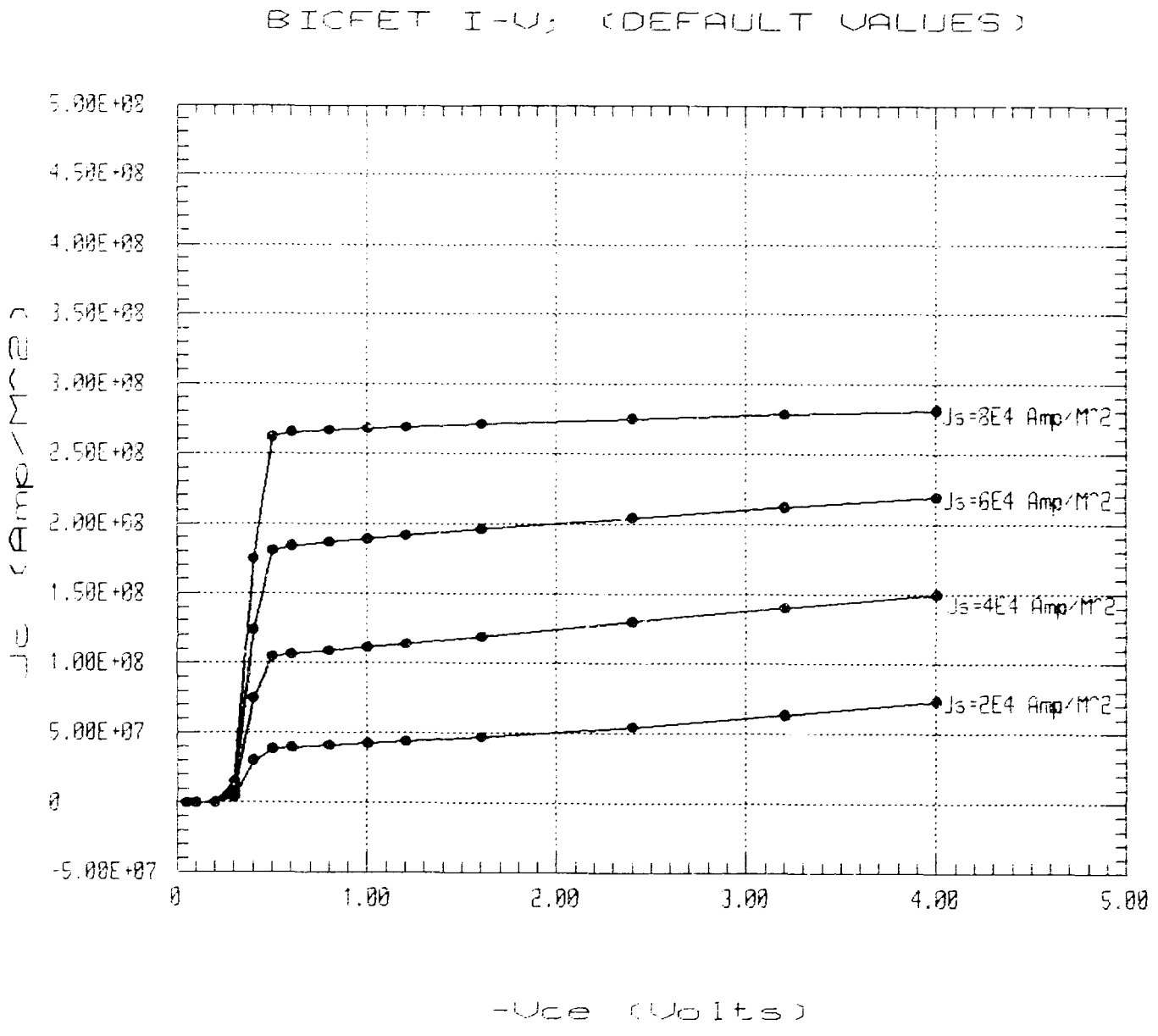


Figure 5.7 Collector current-voltage characteristics for a BICFET with a 350 Å AlGaAs layer

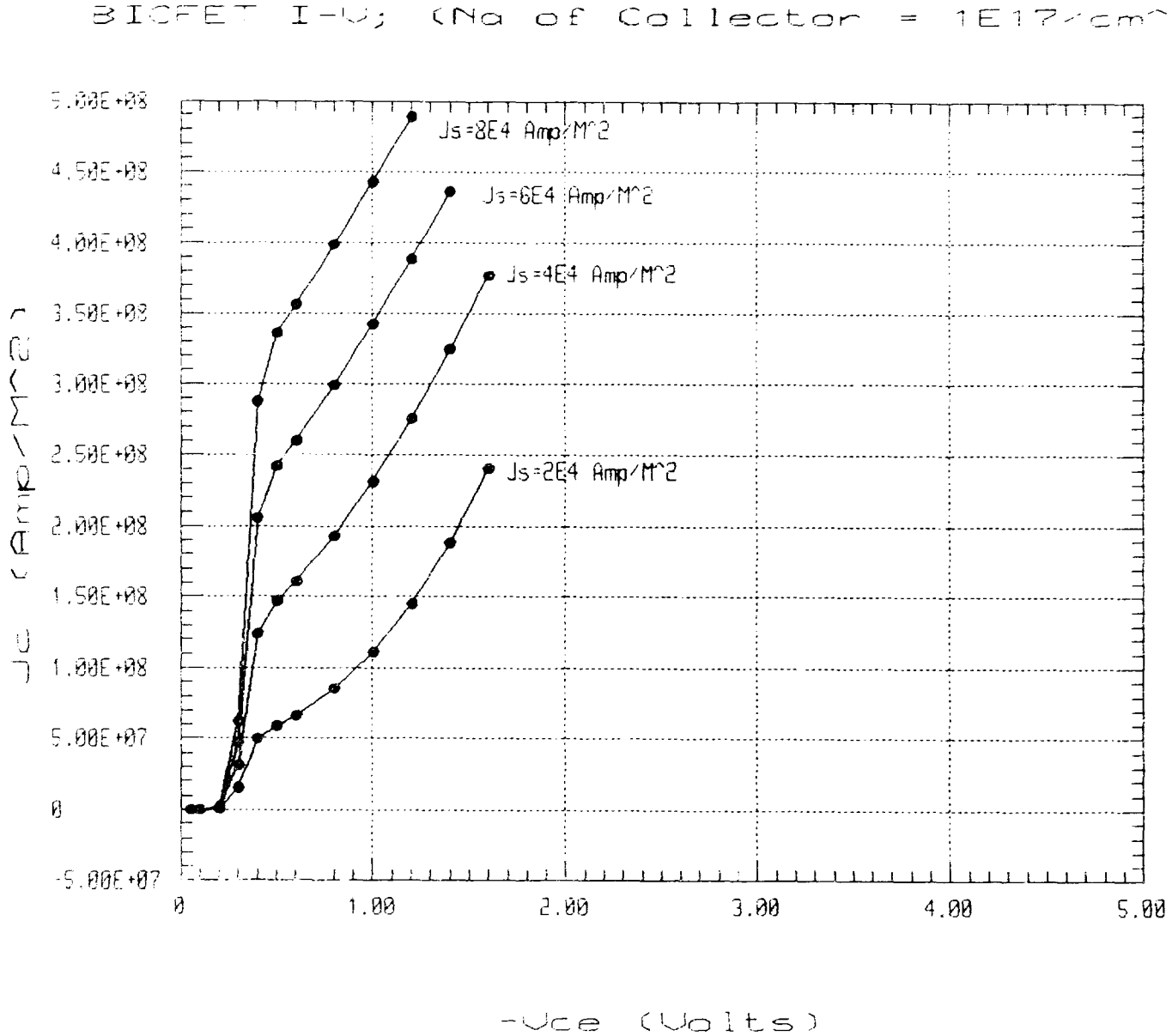


Figure 5.8 Collector current-voltage characteristics for a BICFET with a collector doping concentration of 1×10^{17} cm^{-3}

350 Å AlGaAs layer, a maximum in the conduction band potential occurs near the middle of the layer and is greater than the potential corresponding to the conduction band discontinuity. This enhanced barrier-to-electron flow was used in the analytical formula for calculating the source current J_s. Similarly, the maximum barrier-to-hole flow was used to calculate the effective collector current. However, for holes, the maximum barrier occurs either at one side or the other of the AlGaAs layer. For the 200 Å AlGaAs layer, the maximum of the conduction band potential occurs at the left edge while the maximum of the valence band potential occurs at the right edge. No modifications of the current formulae were made to account for the varying maximum barrier positions. The effects of these variations will be further discussed in Section 5.3.

The collector current-voltage characteristics are shown in Figures 5.6 through 5.8. Figure 5.6 shows the I-V characteristics for the default parameters except that the AlGaAs layer is set at 200 Å. Figure 5.7 shows the characteristics for all default parameters. Figure 5.8 shows the characteristics for the default parameters apart from the collector doping concentration which is set at $1x10^{17}$ cm^{-3}. In Figures 5.6 and 5.7, the collector current density reaches a saturation value at a collector-emitter voltage of about 0.5 V. For the higher collector doping concentration shown in Figure 5.8, poor current saturation takes place and, consequently, this structure is inappropriate for digital or microwave device applications.

For all of the structures investigated, I-V characteristic "cut-in" occurs at V_{ce} = 0.2 to 0.3 V, below which the collector current is negative [21,27]. This effect occurs because the diffusion current component of the collector current given by Eq. (5.11) becomes dominant when V_{ce} is small and consequently the current polarity is reversed. The cut in voltage, however, can be reduced to almost zero if the band gap of the collector is graded from narrow band gap (GaAs) at the interface to wide band gap (AlGaAs) at the depletion edge [21].

Another effect which needs to be considered in the BICFET structure is collector stretching [21]. This effect occurs at high collector

current densities when partial neutralization of the acceptor density in the collector causes an increase in the depletion layer length. Figure 5.7 shows that the curve corresponding to $J_s = 8$ A cm^{-2} has a higher impedance in the saturation region compared with the other three curves. This is a direct effect of collector stretching since the extended collector depletion layer results in a debiasing of the barrier layer, i.e., the biasing effect of V_{ce} is reduced.

It is interesting to note that the current gain in Figure 5.6 is about 100 while the current gain in Figure 5.7 is about 3500. This can be understood from the band diagrams shown in Figures 5.4 and 5.5 and Eq. (5.12). The barrier differences for electrons and holes to overcome in Figure 5.4 is only $\sim (\Delta E_c - \Delta E_v) = 0.131$ eV, while in Figure 5.5, this value is $\sim (\Delta E_c - \Delta E_v + 'E_{hump}') = 0.231$ eV.

The dependence of the current gain on temperature is shown in Figure 5.9. The trend toward higher current gains at low temperatures is similar to that found for HBTs [28].

Although the results presented here predict that the BICFET is capable of high gain performance for the $Al_{0.3}Ga_{0.7}As/GaAs$ material system, we believe that still better performance predictions can be obtained for other structures. In particular, materials with higher values of $(\Delta E_c - \Delta E_v + E_{hump})$ and larger spike doping densities should yield higher values of current gain and collector current.

5.3 ONE-DIMENSIONAL BICFET SIMULATION

5.3.1 Introduction

The semi-analytical theory of the BICFET presented in the last section, was based on a number of assumptions which were listed in Section 5.2.2. These assumptions may not be true in the real case, e.g., zero thickness of the spike layer, complete depletion of the AlGaAs layer and thermionic emission-diffusion transport with its associated

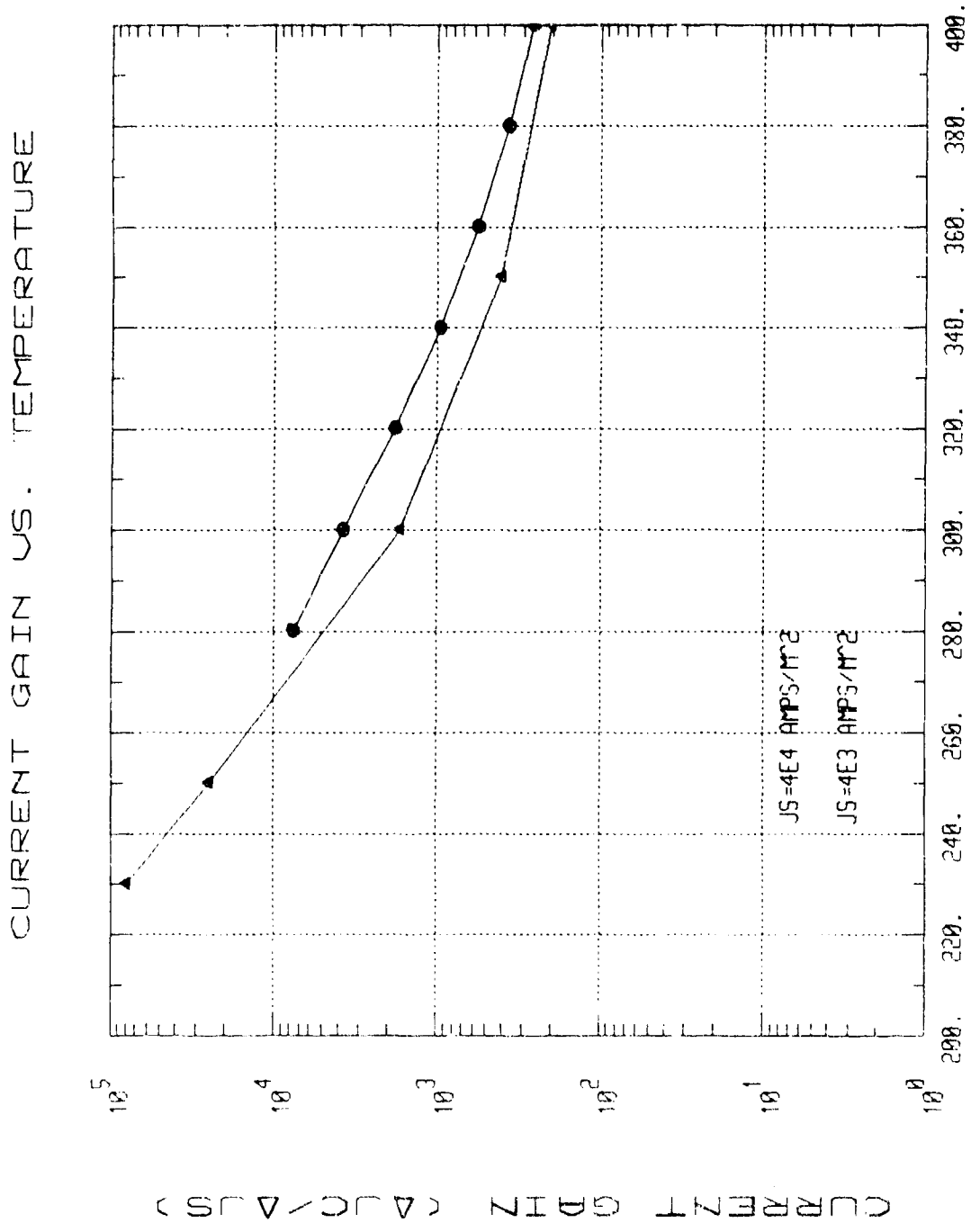


Figure 5.9 Current gain as a function of temperature for two different source currents of a default parameter BICFET

phenomelogical velocity in the SI layer. In order to have a more accurate prediction of BICFET performance, development of a one-dimensional numerical simulation was carried out.

For a full description of the charge transport in a semiconductor device, we need to write down Poisson's and continuity equations for electrons and holes. The variables to be solved from these equations are potential as a function of position, $\phi(x)$, electron concentration as a function of position, $n(x)$, and hole concentration as a function of position, $p(x)$ [29]. The transport equations describing these three variables are coupled and nonlinear and require a numerical scheme to obtain a solution. Generally, it requires a discretization of the entire device structure into mesh points. The values of the unknowns at each mesh point are related to the values of neighboring points. The relation is described by differential equations with a numerical difference scheme replacing the differential operators. These differential equations can then be solved simultaneously to obtain the values of the unknown parameters as a function of space.

5.3.2 Basic Equations for a Homojunction Device in Steady State

The basic equations which describe a semiconductor device are

Poisson's equation

$$\nabla^2\psi = \frac{q}{\epsilon}(n-p-c) \tag{5.18}$$

Continuity equations

$$\nabla \cdot \vec{J}_n - q\frac{\partial n}{\partial t} = qR(\psi, n, p) \tag{5.19}$$

$$\nabla \cdot \vec{J}_p + \frac{\partial p}{\partial t} = -qR(\psi, n, p) \tag{5.20}$$

Current equations

$$\vec{J}_n = -q(\mu_n n \nabla\psi - D_n \nabla n) \tag{5.21}$$

$$\vec{J}_p = -q(\mu_p p \nabla\psi = D_p \nabla p) \tag{5.22}$$

where the symbols are defined as follows

- q - electronic charge
- ε - dielectric constant
- n,p - free electron, hole concentration
- c - net immobile charge density (N_D-N_A)
- $\vec{J}_n, \vec{J}_p$ - electron, hole current density
- R - net recombination rate
- μ_n, μ_p - electron, hole mobility
- D_n, D_p - electron, hole coefficient of diffusion

Under steady-state conditions, i.e., $\partial n/\partial t = \partial p/\partial t = 0$, using the central difference method the equations 5.18, 5.19 and 5.20 can be discretizes in the following forms [10]

$$\psi_{i-1}\frac{\lambda^2}{h_{i-1}} - \psi_i\lambda^2\left[\frac{1}{h_i} + \frac{1}{h_{i-1}}\right] + \psi_{i+1}\frac{\lambda^2}{h_i} = (n_i - p_i - c_i)\frac{h_i + h_{i-1}}{2} \tag{5.23}$$

$$n_i \frac{D_{n|i-1/2}}{h_{i-1}} B\left(\frac{\psi_{i-1}-\psi_i}{U_t}\right) - n_i\left[\frac{D_{n|i-1/2}}{h_{i-1}} B\left(\frac{\psi_i - \psi_{i-1}}{U_t}\right) + \frac{D_{n|i+1/2}}{h_{i-1}} B\left(\frac{\psi_i - \psi_{i+1}}{U_t}\right)\right]$$

$$+ n_{i+1}\frac{D_{n|i+1/2}}{h_i} B\left(\frac{\psi_{i+1}-\psi_i}{U_t}\right) = R_i\left(\frac{h_{i-1}+h_i}{2}\right) \tag{5.24}$$

$$p_i \frac{D_{p|i-1/2}}{h_{i-1}} B\left(\frac{\psi_i - \psi_{i-1}}{U_t}\right) - p_i\left[\frac{D_{p|i-1/2}}{h_{i-1}} B\left(\frac{\psi_{i-1}-\psi_i}{U_t}\right) + \frac{D_{p|i+1/2}}{h_i} B\left(\frac{\psi_{i+1} - \psi_i}{U_t}\right)\right]$$

$$+ p_{i+1}\frac{D_{p|i+1/2}}{h_i} B\left(\frac{\psi_i - \psi_{i+1}}{U_t}\right) = R_i\left(\frac{h_{i-1}+h_i}{2}\right) \tag{5.25}$$

where

$$\lambda^2 = \varepsilon/q \tag{5.26}$$

$$U_t = kT/q \tag{5.27}$$

$$B(x) = x/(e^x-1) \tag{5.28}$$

$$R_i = (n_i p_i - N_i^2)/[\tau_p(n_i+N_i) + \tau_n(p_i+N_i)] \tag{5.29}$$

τ_n and τ_p are life times of electrons and holes, respectively, in the Shockley-Read-Hall (S-R-H) generation-recombination equation, and Ni is assumed to be the intrinsic carrier concentration. Once $\psi(x)$, $n(x)$, and $p(x)$ are solved for each discretized point, $J_n(x)$ and $J_p(x)$, can be calculated from the following equations:

$$J_n|_{i+1/2} = \frac{D_n|_{i+1/2}}{h_i}\left[n_i B\left(\frac{\psi_i - \psi_{i+1}}{U_t}\right) - n_{i+1} B\left(\frac{\psi_{i+1} - \psi_i}{U_t}\right)\right] \tag{5.30}$$

$$J_p|_{i+1/2} = \frac{D_p|_{i+1/2}}{h_i}\left[p_{i+1} B\left(\frac{\psi_i - \psi_{i+1}}{U_t}\right) - p_i B\left(\frac{\psi_{i+1} - \psi_i}{U_t}\right)\right] \tag{5.31}$$

The boundary conditions are determined by the applied votages at terminals of the devices. For current modulation devices such as bipolar transistors operated in the common-emitter mode, a current boundary condition needs to be specified at the injection terminal. For the most simple case of a p-n junction, the boundary conditions are specified in the following:

$$\psi(X_p) = \psi_b(N_a) + V_p \quad ; \quad \psi(X_n) = \psi_b(N_d) + V_n$$

$$p(X_p) = N_a \quad ; \quad p(X_n) = N_i^2/N_d \tag{5.32}$$

$$n(X_p) = N_i^2/N_a \quad ; \quad n(X_n) = N_d$$

where X_n and X_p are the contact positions at the n and p terminals, respectively. N_a and N_d are the doping concentration in the p and n regions, respectively. ψ_b is the built-in potential. V_p and V_n are the applied biases at the p and n contacts, respectively. The boundary conditions for the n and p layers are obtained by assuming that the surface recombination velocities are infinite at the ohmic contacts. This is equivalent to saying that the quasi fermi levels coincide with the fermi levels at the ohmic contacts. For a p-n-p bipolar transistor, the boundary conditions are specified as follows [30]

$$\psi(X_e) = \psi_b(N_{ae}) = V_e \quad ; \quad \psi(X_c) = \psi_b(N_{ac}) + V_c$$

$$p(X_e) = N_{ae} \quad ; \quad p(X_c) = N_{ac} \tag{5.33}$$

$$N(X_e) = N_i^2/N_{ae} \quad ; \quad N(X_c) = N_i/N_c^{\,2}$$

$$\phi_n(X_b) = V_b$$

where X_e, X_b, and X_c are the positions of the emitter, base and collector contacts, respectively. N_{ae} and N_{ac} are the doping concentrations in the emitter and collector regions, respectively. V_e and V_c are the applied voltages at the emitter and collector, respectively. ϕ_n is the quasi-fermi level of electrons.

Once the boundary conditions are specified, the task is then to solve a large system of equations. This system contains N discretized Poisson's equations, N discretized electron continuity equations, and N discretized hole continuity equations. A numerical method is required to solve these equations.

5.3.3 Basic Equations for a Heterojunction Device in Steady State

In ordinary homojunction device modeling, the following factors are included in the transport equations,

1. Drift and diffusion currents
2. Position dependent doping
3. Doping and field dependent mobility
4. Generation and recombination effects

The introduction of spatially varying composition requires the following additional factors [31]:

1. Position-dependent bandgap
2. Position-dependent electron affinity
3. Position-dependent dielectric constant
4. Position-dependent effective carrier density in conduction and valence bands
5. Other position-dependent parameters such as mobility and carrier life time.
6. Carrier transport mechanism other than drift and diffusion, such as tunneling, thermionic-field emission and hot-electron injecion.

Successful modeling depends on the use of correct material-dependent parameters and transport mechanisms. The modeling of heterojunction devices at this stage considers only the diffusion and drift components of carrier transport. The drift component comes from the gradient of the electrostatic potential, as well as the built-in field due to the position-varying band energy. The diffusion component comes from the gradient of carrier concentrations as well as the gradient of the effective density of states [32]. The equations describing the electron and hole concentrations are [33]

$$n = \omega n_i \exp\left[\frac{q(\psi-\phi_n)}{kT}\right] \tag{5.34}$$

$$p = \frac{n_i}{\omega} \exp \frac{q(\phi_p - \psi)}{kT} \tag{5.35}$$

where

$$n_i = [N_C(x)N_V(x)]^{1/2} \exp\left[\frac{-E_g(x)}{2kT}\right] \tag{5.36}$$

$$\omega = \left[\frac{N_V^{(0)} N_C(x)}{N_C^{(0)} N_V(x)}\right]^{1/2} \exp\left[\frac{E_g(x) - E_g^{(0)}}{2kT}\right] \exp\left[\frac{\chi(x) - \chi^{(0)}}{kT}\right] \tag{5.37}$$

where E_g and χ denote the band gap and electron affinity, respectively N_c and N_v are the equivalent density of states in the conduction and valence bands, respectively. ψ is the electrostatic potential, and ϕ_n and ϕ_p are the quasi-fermi levels for electrons and holes, respectively. The quantities with zero superscripts represent those arbitrary reference points. The current densities for electrons and holes, given by Eqs. (5.21) and (5.22) can be written as

$$\vec{J}_n = -q\ \mu_n n \nabla\phi_n = q\ D_n \nabla n + q\ \mu_n \vec{E}_n n \tag{5.38}$$

$$\vec{J}_p = -q\ \mu_p p \nabla\phi_p = -q\ D_p\ \nabla p + q\ \mu_n \vec{E}_p p \tag{5.39}$$

where

$$\vec{E}_n = \vec{E} - \frac{kT}{q} \nabla\ [\ln(\omega n_i)] \tag{5.40}$$

$$\vec{E}_p = \vec{E} - \frac{kT}{q} \nabla\ [\ln(\omega n_i)] \tag{5.41}$$

and

$$\vec{E} = -\nabla\psi \tag{5.42}$$

The boundary conditions for potentials at emitter and collector ohmic contacts are

$$\psi(X_i) = V(X_i) + \frac{kT}{q} \ln\left[\frac{n(X_i)}{\omega(X_i)n_i(X_i)}\right] \tag{5.43}$$

$$\phi_n(X_i) = V(X_i) \tag{5.44}$$

$$\phi_p(X_i) = V(X_i) \tag{5.45}$$

where X_i is either the emitter or collector contact point. The boundary condition at the base is specified as either

$$\phi_n(X_b) = V(X_b) \tag{5.46}$$

or

$$\phi_p(X_b) = V(X_b) \tag{5.47}$$

depending on whether n or p type carriers are being injected into the base.

5.3.4 Results and Discussion

The computer codes were written to solve the discretized coupled nonlinear transport equations described in the previous sections. The method used was a coupled-solution with the Gaussian-Seidel iteration scheme. The existing program has some assumptions and limitations, which are listed as follows:

1. One-dimensional intrinsic device simulation
2. Maxwell-Boltzman statistics used
3. Dirichlet boundary condition, i.e., boundary conditions are specified by electrostatic potential rather than by current
4. The mobility is a constant throughout the device
5. Steady state calculation
6. Low to moderate injection levels
7. The generation recombination mechanism includes only S-R-H
8. Time-consuming calculation

The basic structure of a BICFET is essentially a single heterojunction bipolar transistor with a thin heavily-doped base. The typical base width in a SHBT is of the order of 1000 Å, while in a BICFET, this width is $\leq$50 Å. A series of structures was studied in order to determine the trend of transistor behavior leading from SHBT to BICFET. There are four structures, #A, #B, #C, and #D, in the simulation study. Their structures are described below:

Structure #A:

p^+GaAs, 5E18/cm^3, 0.04 μm
pAlGaAs, 5E17/cm^3, 350 Å
n^+GaAs, 5E18/cm^3, 50 Å
pGaAs, 2E16/cm^3 0.7, μm
p^+GaAs, 5E18/cm^3, 0.04 μm

Structure #B:

p^+GaAs, 5E18/cm^3, 0.04 μm
pAlGaAs, 1E17/cm^3, 750 Å
n^+GaAs, 5E18/cm^3, 50 Å
pGaAs, 2E16/cm^3, 0.8 μm
p^+GaAs, 5E18/cm^3, 0.04 μm

Structure #C:

p^+GaAs, 5E18/cm^3, 0.04 μm
pAlGaAs, 5E17/cm^3, 350 Å
n^+GaAs, 5E18/cm^3, 200 Å
pGaAs, 2E16/cm^3, 0.8 μm
p^+GaAs, 5E18/cm^3, 0.04 μm

Structure #D:

p^+GaAs, 5E18/cm^3, 0.04 μm
pAlGaAs, 5E17/cm^3, 350 Å
n^+GaAs, 5E18/cm^3, 1000 Å
pGaAs, 2E16/cm^3, 0.8 μm
p^+GaAs, 5E18/cm^3, 0.04 μm

Structures #A and #B are basic BICFET structures. #C and #D are SHBT structures similar to #A except that the base/source width are 200 Å and 1000 Å, respectively. The mobilities for electron and hole were assumed to be 4000 and 400 cm^2/volts/sec, respectively, throughout the structure.

Figure 5.10 shows the simulated J_C vs $-V_{CE}$ characteristics for #A. The different curves correspond to different applied biases between the source and emitter. For $-V_{CE}$ larger than 0.4 volts, the source current density, J_B, is approximately constant. This behavior of J_C vs $-V_{CE}$ is essentially the same for all the rest of the structures. Figure 5.11 shows J_C and J_B vs $-V_{BE}$ at V_{CE} = - 1.0 volts for all

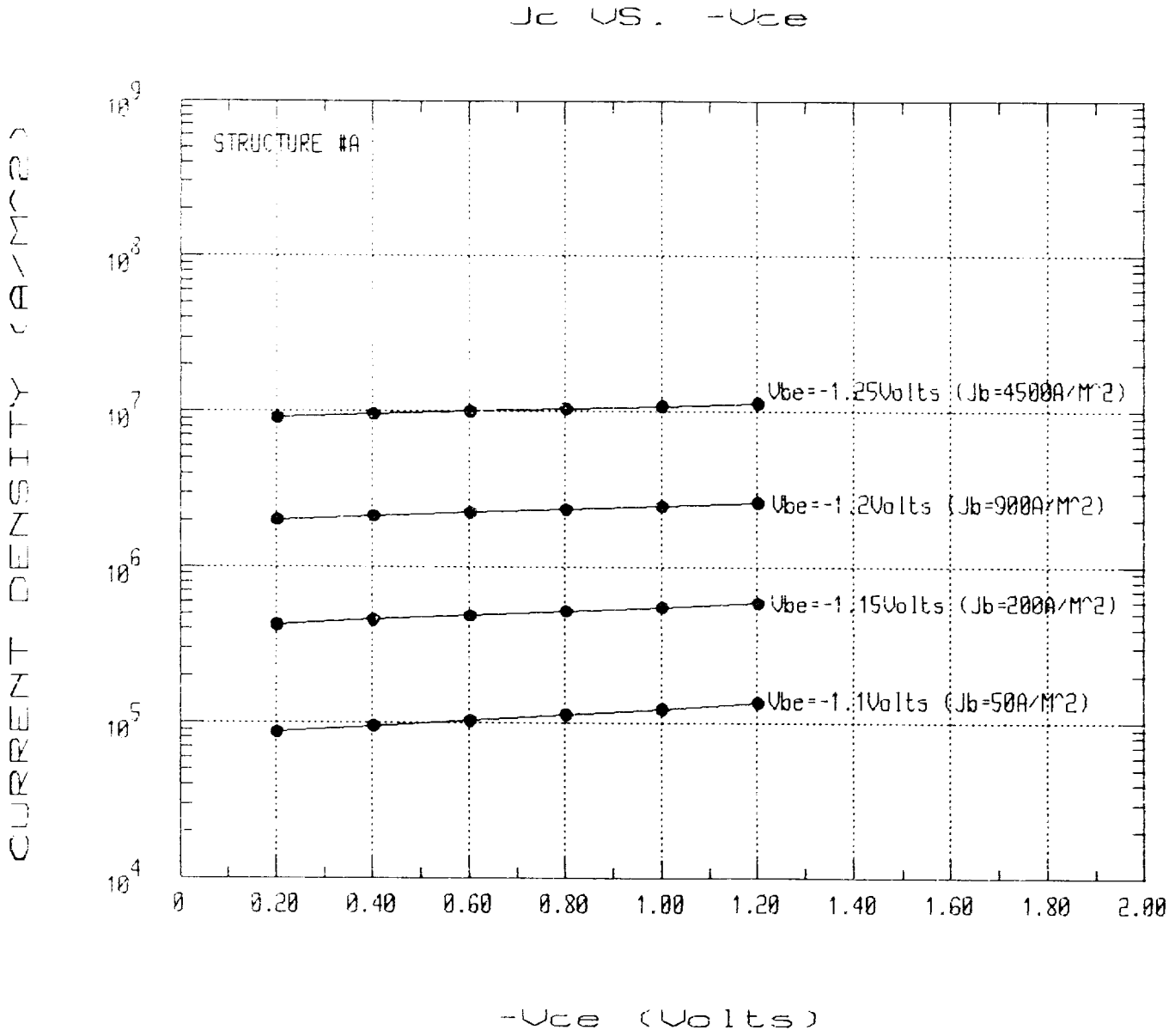


Figure 5.10 Collector current-voltage characteristics for a structure #A BICFET

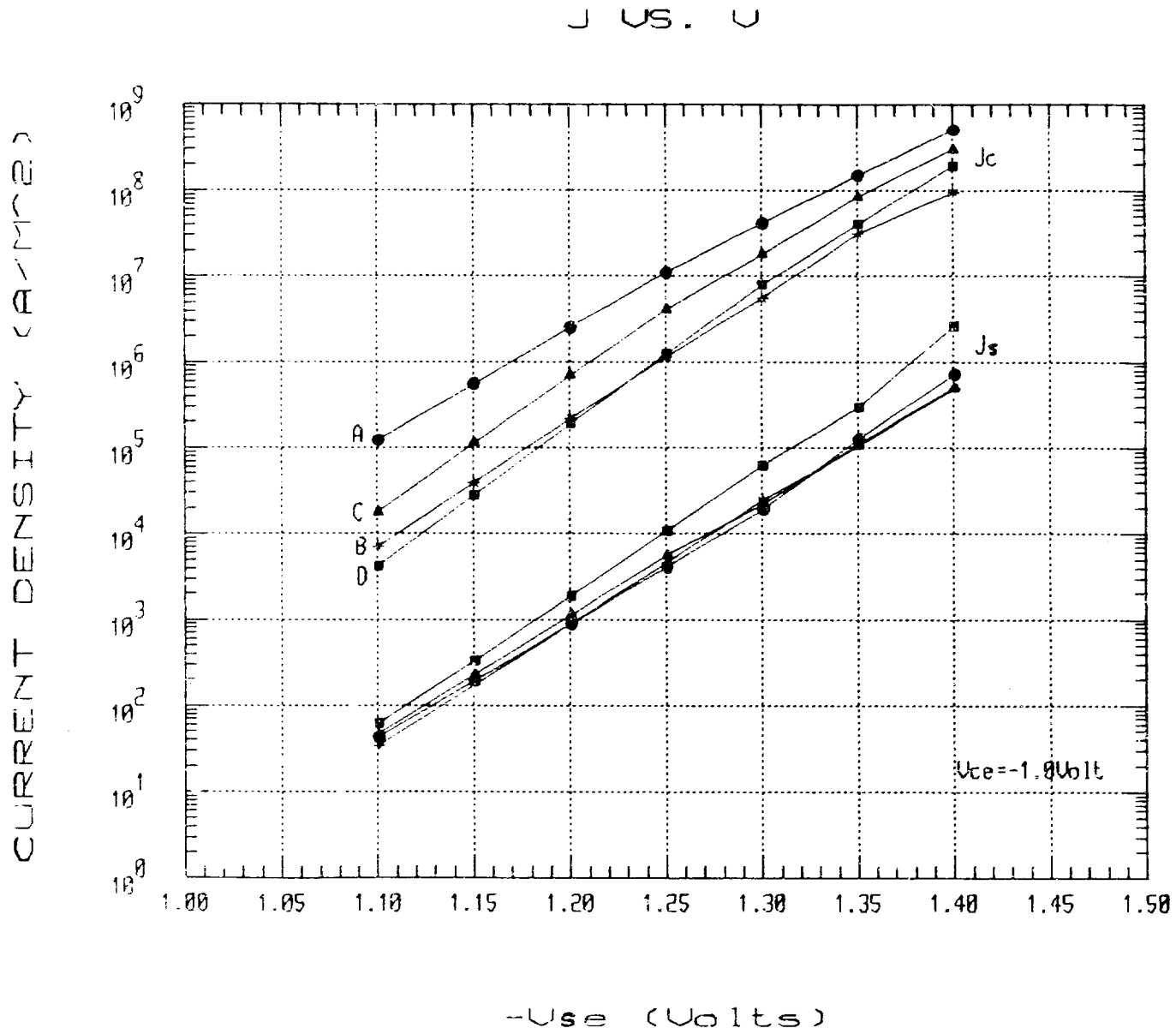


Figure 5.11 Collector and source current as a function of source-emitter voltage for BICFET structures #A, #B, #C and #D

the structures. Figure 5.12 shows the current gain, β as a function of emitter current, J_C, at V_{CE} = - 1.0 volts.

The slopes of both sets of curves in Figure 5.11 show an ideality factor close to unity in the lower part of the V_{BE} range between -1.1 volts and -1.4 volts. As the bias increases, the ideality factor increases. This indicates a tendency toward high injection behavior at the upper part of the range studied. Figure 5.12 shows that structure #A has the highest current gain among the four. The fact that the order of decreasing current gain is #A, #B, and #C indicates that as the width of base increases, the current gain decreases. This result is reasonable, since the transport factor is inversely proportional to the width of the base/source. BICFET structure #B, however, shows less current gain than #A. This result becomes clear when we compare the band diagram and carrier distributions of these two structures under bias.

The band diagram and carrier distribution for #A at thermal equilibrium are shown in Figures 5.13 and 5.14, respectively. The band diagram and carrier distribution for #A under bias of V_{ce} = - 1.0 volt and V_{be} = - 1.25 volts are shown in Figures 5.15 and 5.16, respectively.

The band diagram and carrier distribution for #B at thermal equilibrium are shown in Figures 5.17 and 5.18, respectively. The same quantities for #B under bias of V_{ce} = -1.0 volts and V_{be} = -1.25 volts are shown in Figures 5.19 and 5.20, respectively. Comparing the hole distributions shown in Figures 5.16 and 5.20, we see that #A has a greater hole gradient in the SI region than #B, while the electron gradients are about the same. Consequently, the low current gain in structure #B compared with #A may be attributed to this difference. Comparing the band diagrams shown in Figures 5.15 and 5.19, the barrier differences for electrons and holes are about the same for both structures #A and #B under bias. In fact, the band diagrams of the corresponding structure shown in Section 5.2.5 are very similar to the ones shown here.

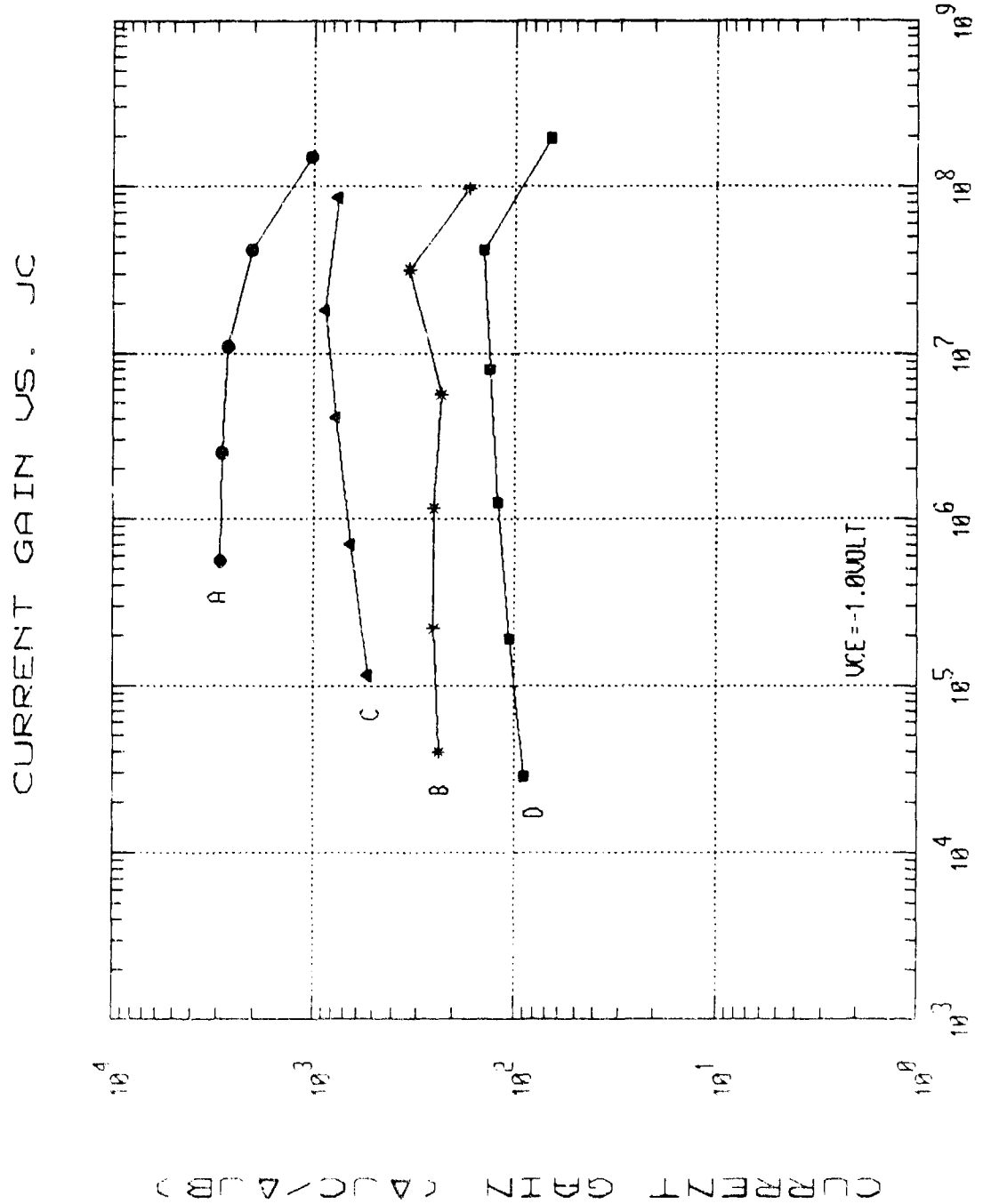


Figure 5.12 Current gain as a function of collector current for BICFET structures #A, #B, #C and #D

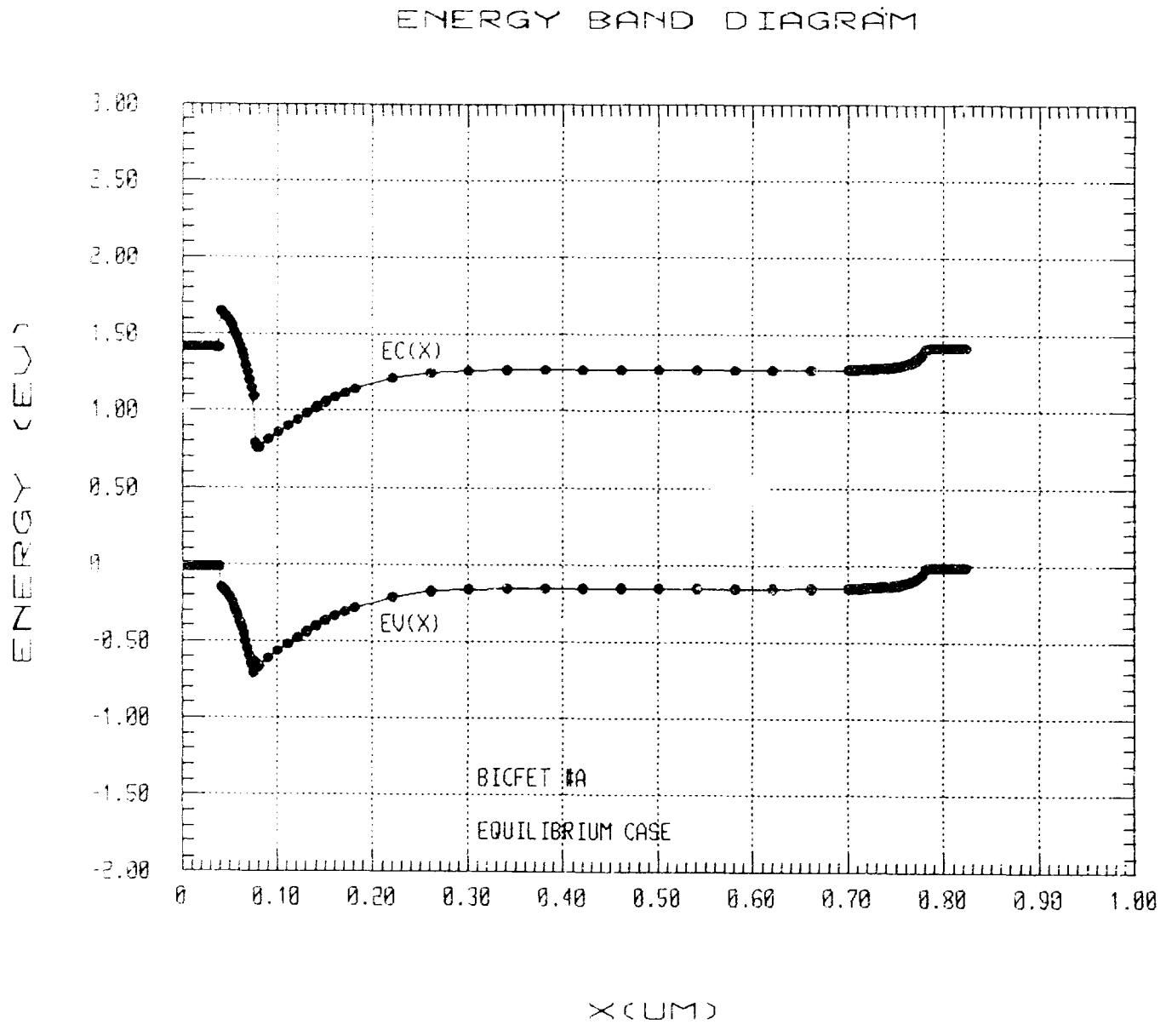


Figure 5.13 Band diagram for BICFET structure #A at equilibrium

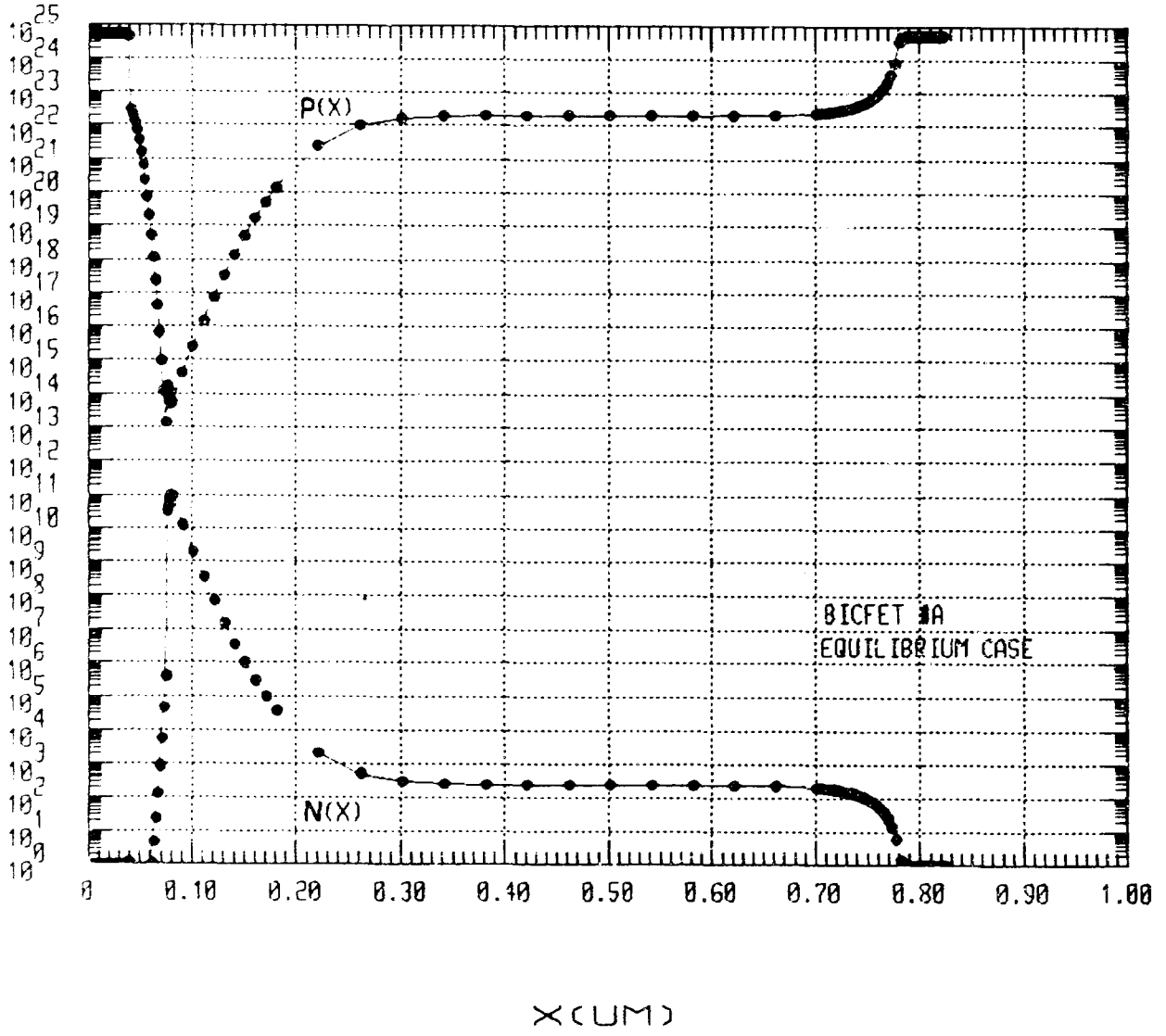


Figure 5.14 Carrier concentration distributions for BICFET structure #A at equilibrium

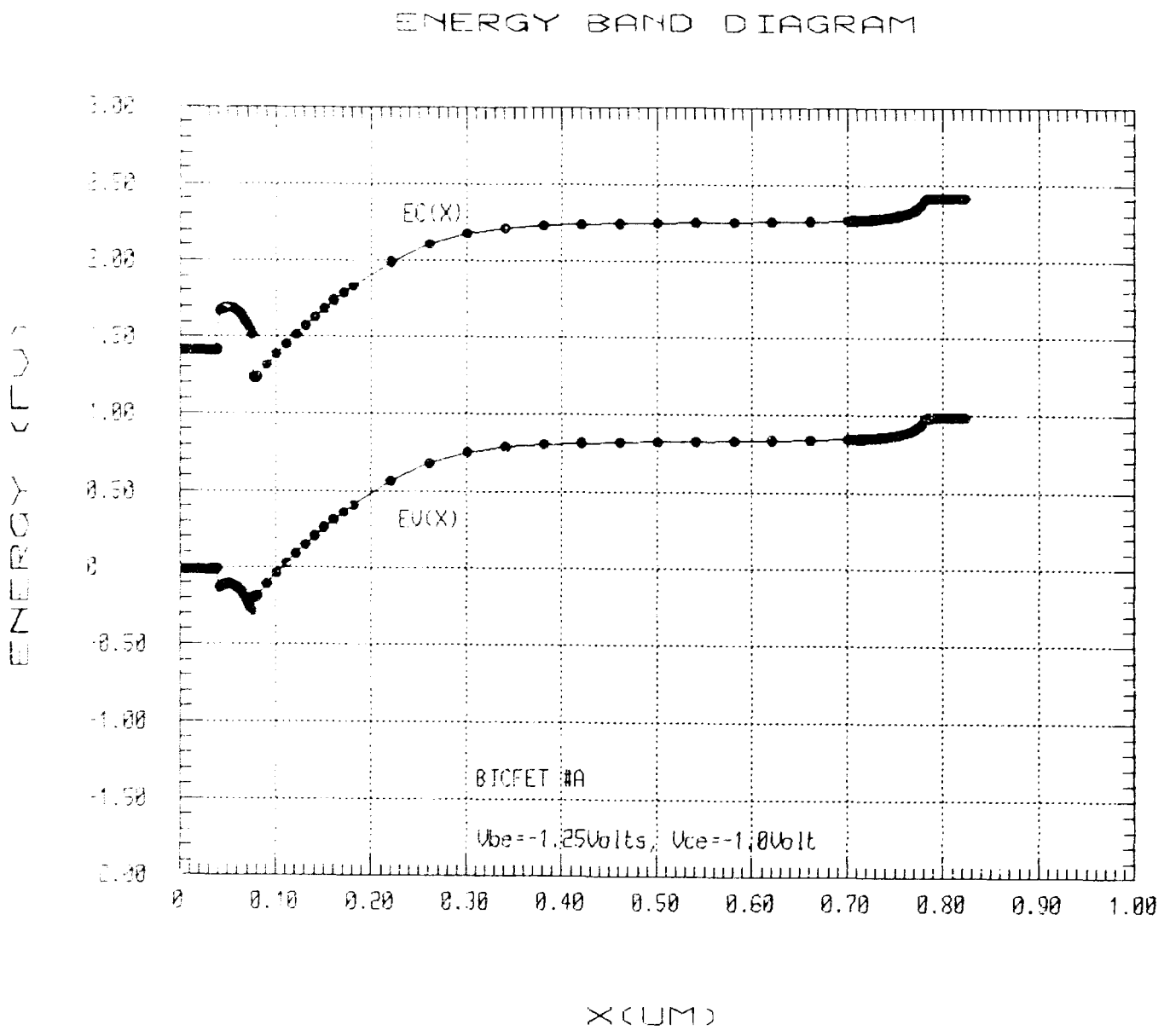


Figure 5.15 Band diagram for BICFET structure #A under bias

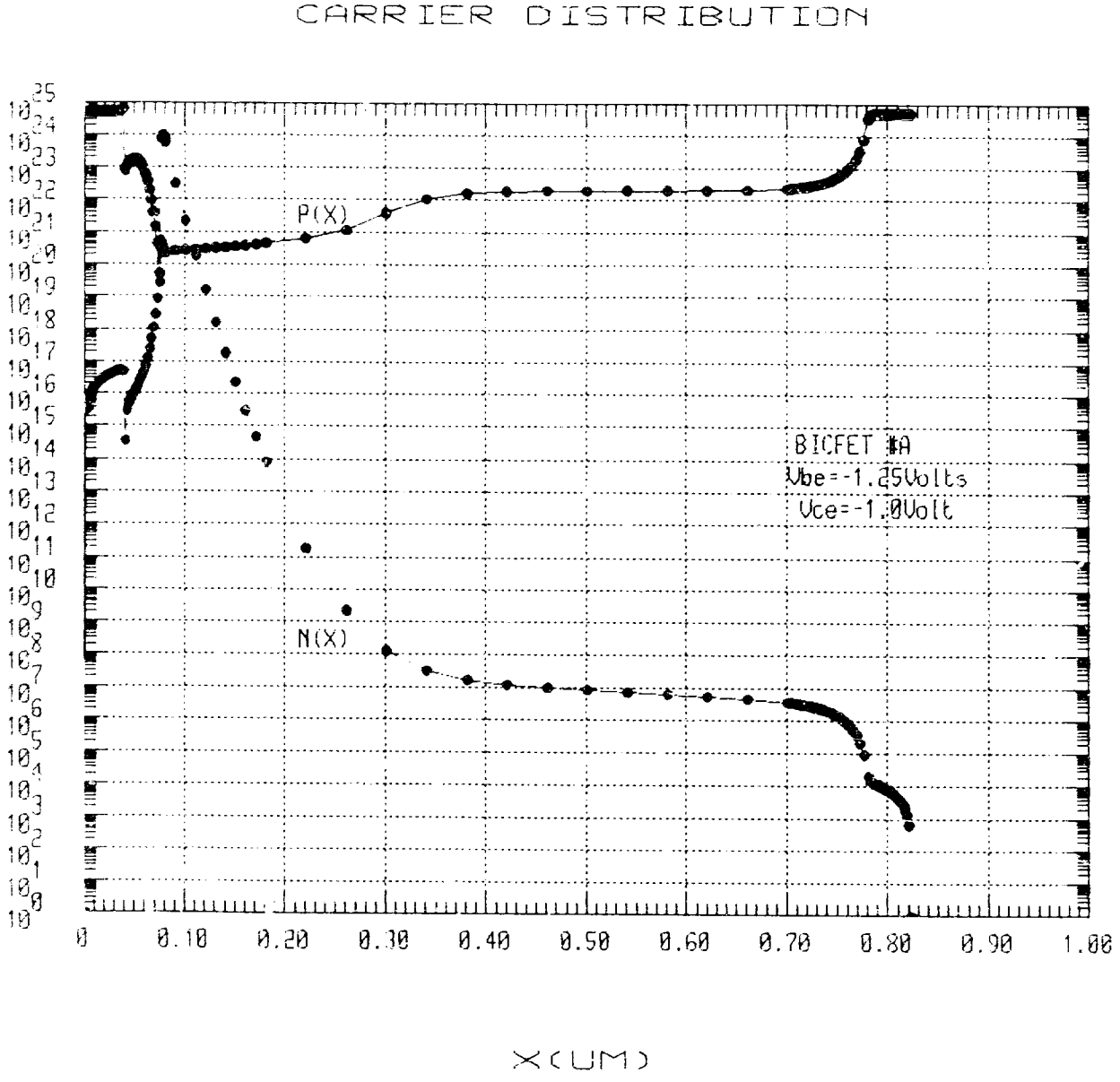


Figure 5.16 Carrier concentration distributions for BICFET structure #A under bias

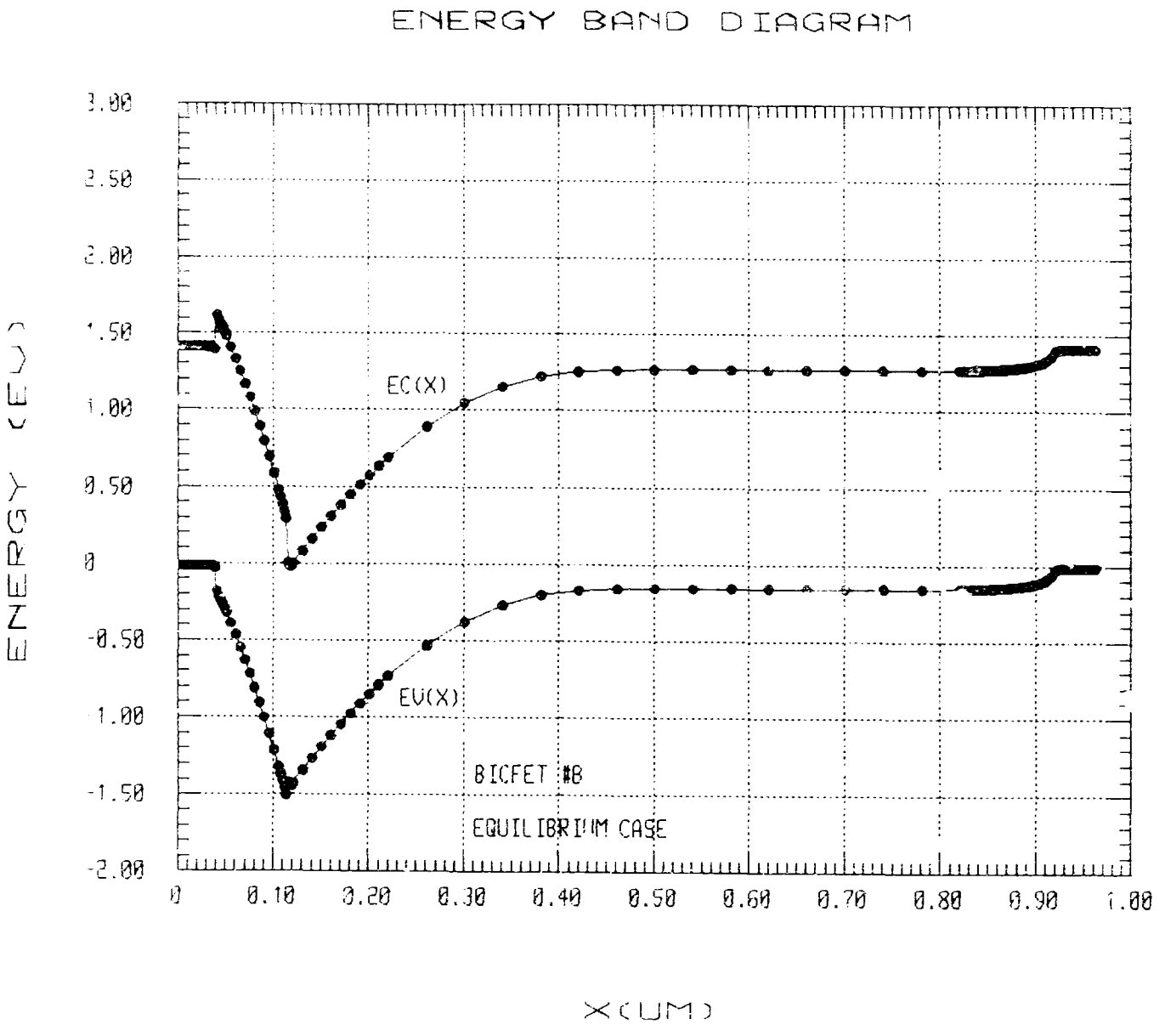


Figure 5.17 **Band diagram for BICFET structure #8 at equilibrium**

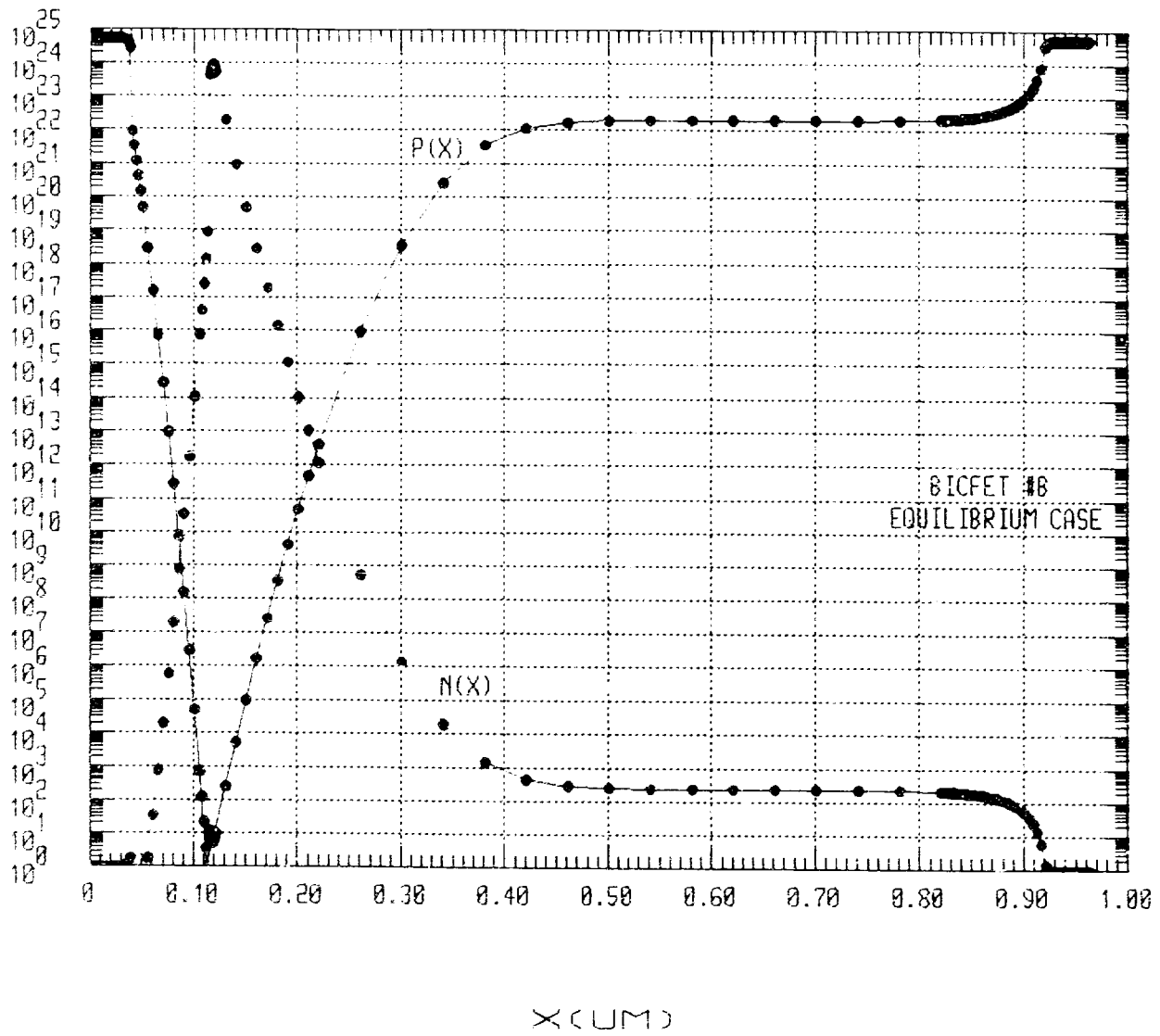


Figure 5.18 Carrier concentration distributions for BICFET structure #B at equilibrium

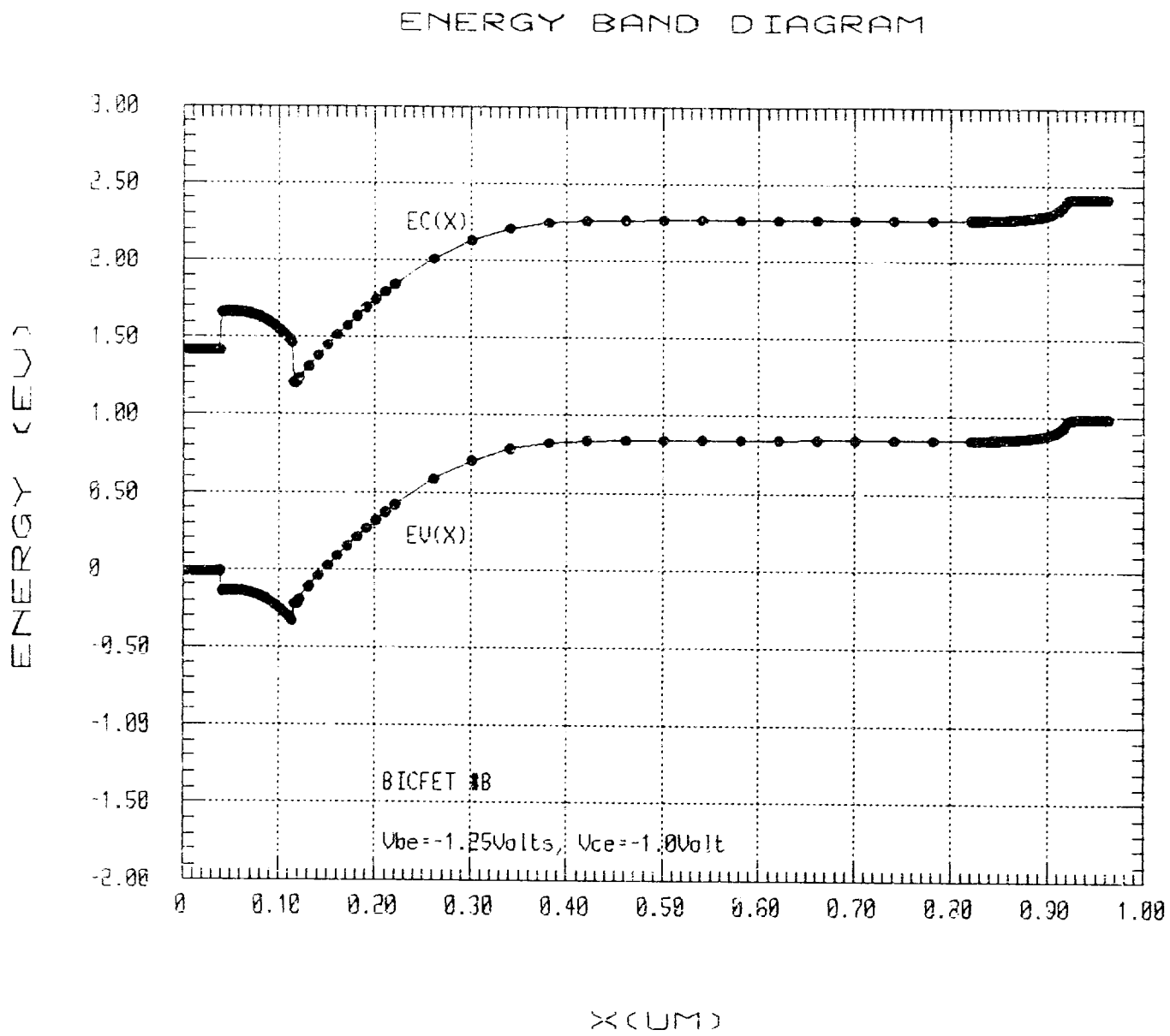


Figure 5.19 Band diagram for BICFET structure #B under bias

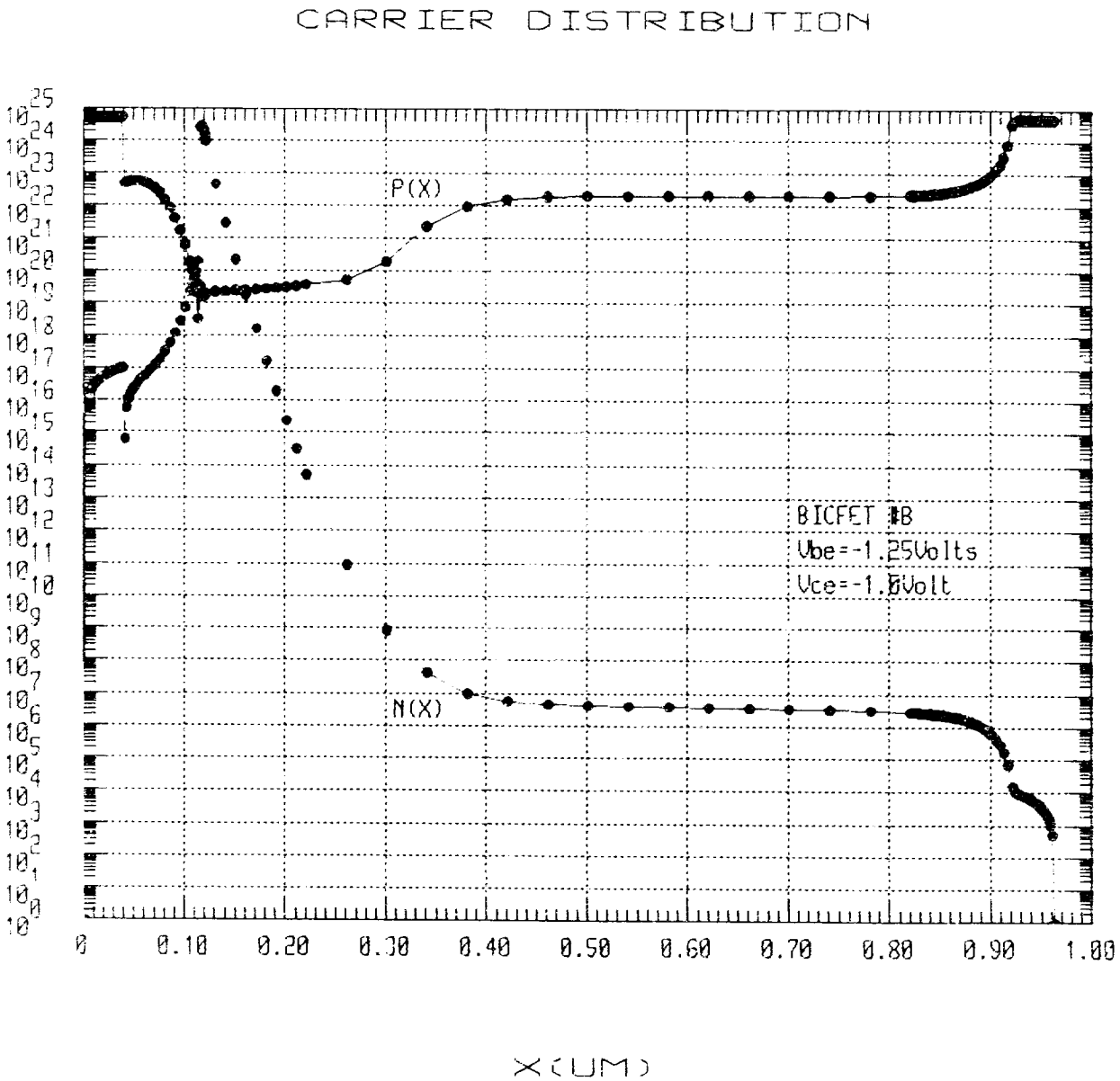


Figure 5.20 Carrier concentration distributions for BICFET structure #B under bias

The following table shows the comparison between the results obtained by using semi-analytical (S-A) and numerical-simulation (N-S) modeling.

	Structure #A		Structure #B	
	S-A	N-S	S-A	N-S
Vbe (Volts)	-1.44	-1.32	-1.40	-1.32
Vce (Volts)	-1.0	-1.0	-1.0	-1.0
Jb (A/M^3)	4.0E4	4.0E4	4.0E4	4.1E4
Jc (A/M^3)	1.1E8	8.8E7	2.3E7	1.23E7
N_o ($/M^3$)	5.90E24	1.2E24	1.05E25	2.2E24
Beta	2800	2200	570	300

Generally, results for both #A and #B show good agreement. However, current gain for #B using the S-A method appears to be considerably higher than predicted by the N-S technique. This might be due to the use of overestimated equivalent carrier velocities in the SI layer of structure #B where the width is large compared to the diffusion length (Eq. 5.12).

The gain has a dependence on the energy barrier difference for electrons and holes as has been discussed in Section 5.25. Depending on the width and doping concentration in the SI layer, a "hump" may form in the conduction band when appropriate voltages are applied to the base and collector relative to the emitter. The existence of a hump in the conduction band increases the barrier for electrons, but not for holes, and, therefore, the current gain is greater for the pnp structure with a hump band structure. This effect introduced in the semi-analytical method is based on the assumption of complete depletion in the wide band gap material.

In order to verify the results shown in Section 5.2.5, four structures were analyzed with the numerical simulation. One of these four structures is the same as Structure #A described above. The other three structures have the same structure parameters apart from the width of the SI layer. The four SI layer thicknesses evaluated are 200 Å,

350 Å, 500 Å, and 750 Å all with a p-type doping concentration of 5E17 cm^{-3}. The table below shows some of the results obtained from the numerical simulation.

	#E	#A	#F	#G
SI width (Å)	200	350	500	750
SI doping (cm^{-3})	5E17	5E17	5E17	5E17
V_{be}(Volts)	-1.25	-1.25	-1.25	-1.25
V_{ce}(Volts)	-1.0	-1.0	-1.0	-1.0
J_b(A/M^2)	2.87E4	4.03E3	2.06E3	2.57E3
J_c(A/M^2)	5.94E6	1.08E7	8.95E6	1.83E7
Beta(J_c/J_b)	207.	2687.	4344.	7124.

The table above shows that J_b is one order of magnitude larger for #E than for the other three structures, and this accounts for the low current gain of #E. Figures 5.21 and 5.22 show the band diagram and carrier concentration distributions for structure #E under bias. Th same quantities for #G under the same bias are shown in Figures 5.23 and 5.24. It is clear that there is no hump in the conduction band for the structure with a 200 Å SI layer thickness (Figure 5.21). The same structure shows an electron concentration in the emitter region (Figure 5.22) of about $1E18M^{-3}$), and that accounts for the high J_b shown in the table.

The band diagram of #A with a 350 Å SI layer thickness (Figure 5.15) shows a hump and the electron concentration in the emitter region (Figure 5.16) is about $1E17M^{-3}$, which accounts for the low J_b. These results seem to agree with those derived using the semi-analytical method where complete depletion and thermionic-emission diffusion transport are assumed. The band diagram for structure #G with a 750 Å SI layer thickness (Figure 5.23) shows a flat region which is undepleted. Therefore, the complete depletion assumption cannot be applied to this structure, although this structure shows a higher dc current gain than the one originally proposed, i.e., structure #A.

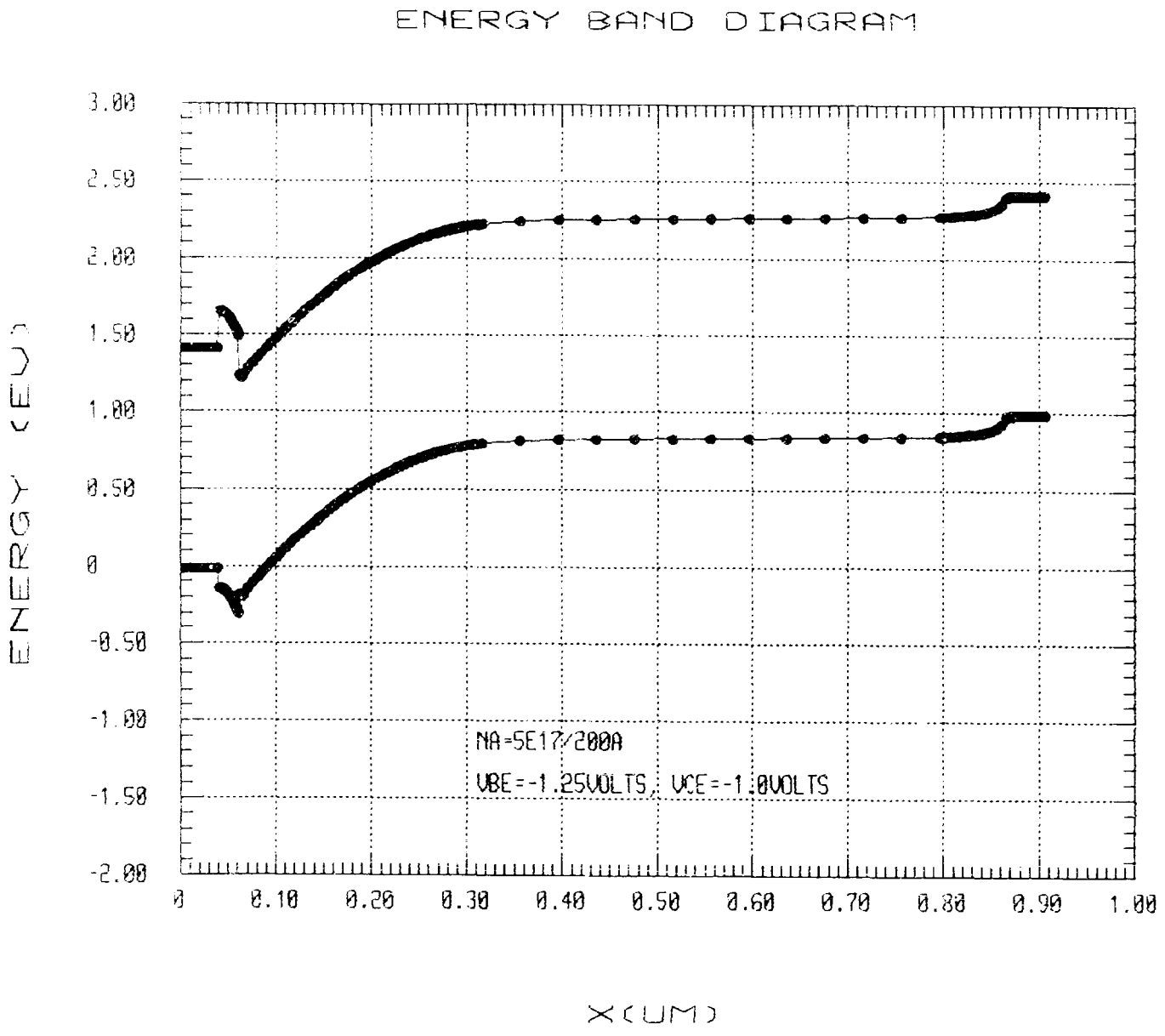


Figure 5.21 Band diagram for BICFET structure #E under bias

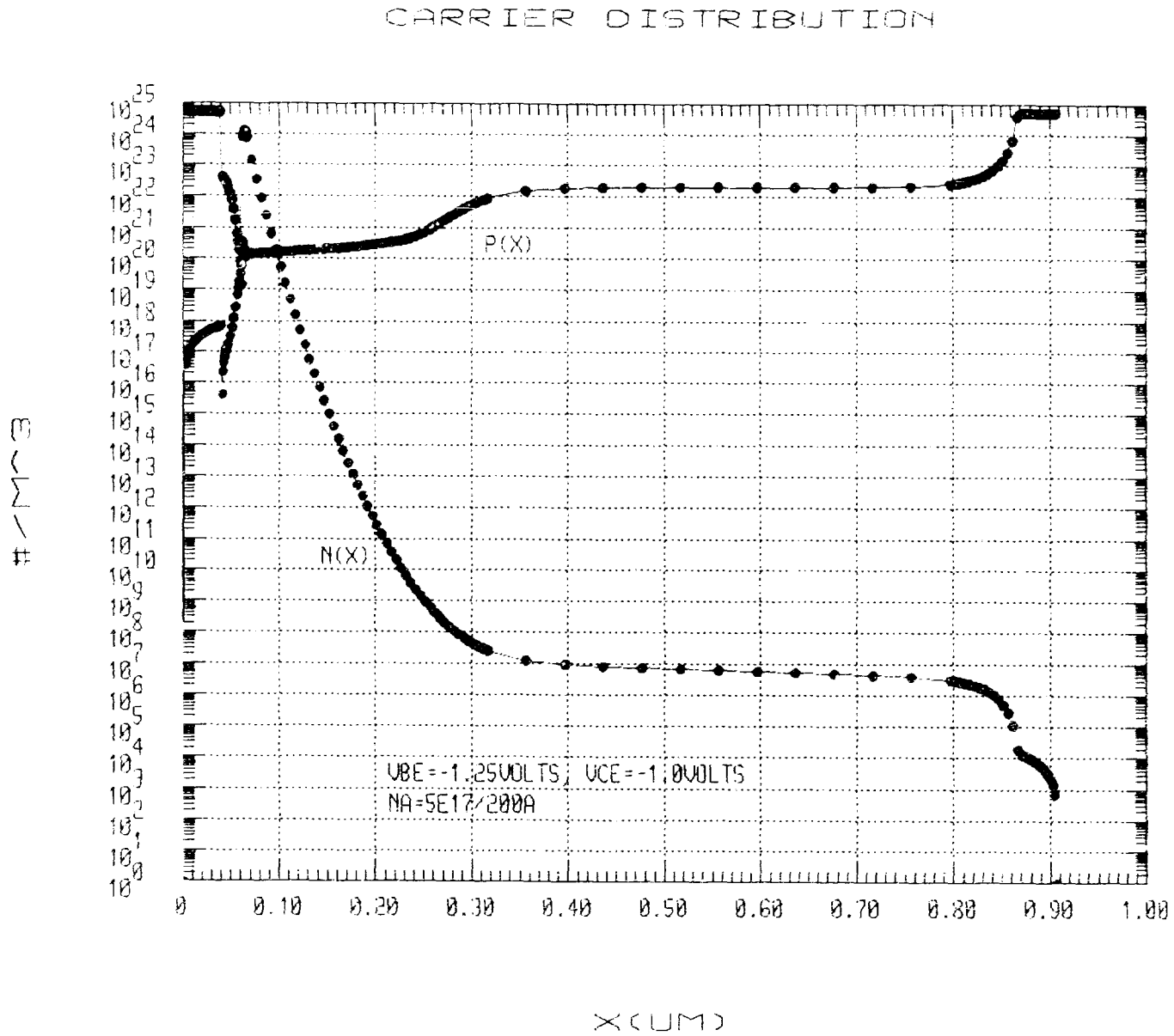


Figure 5.22 Carrier concentration distributions for BICFET structure #E under bias

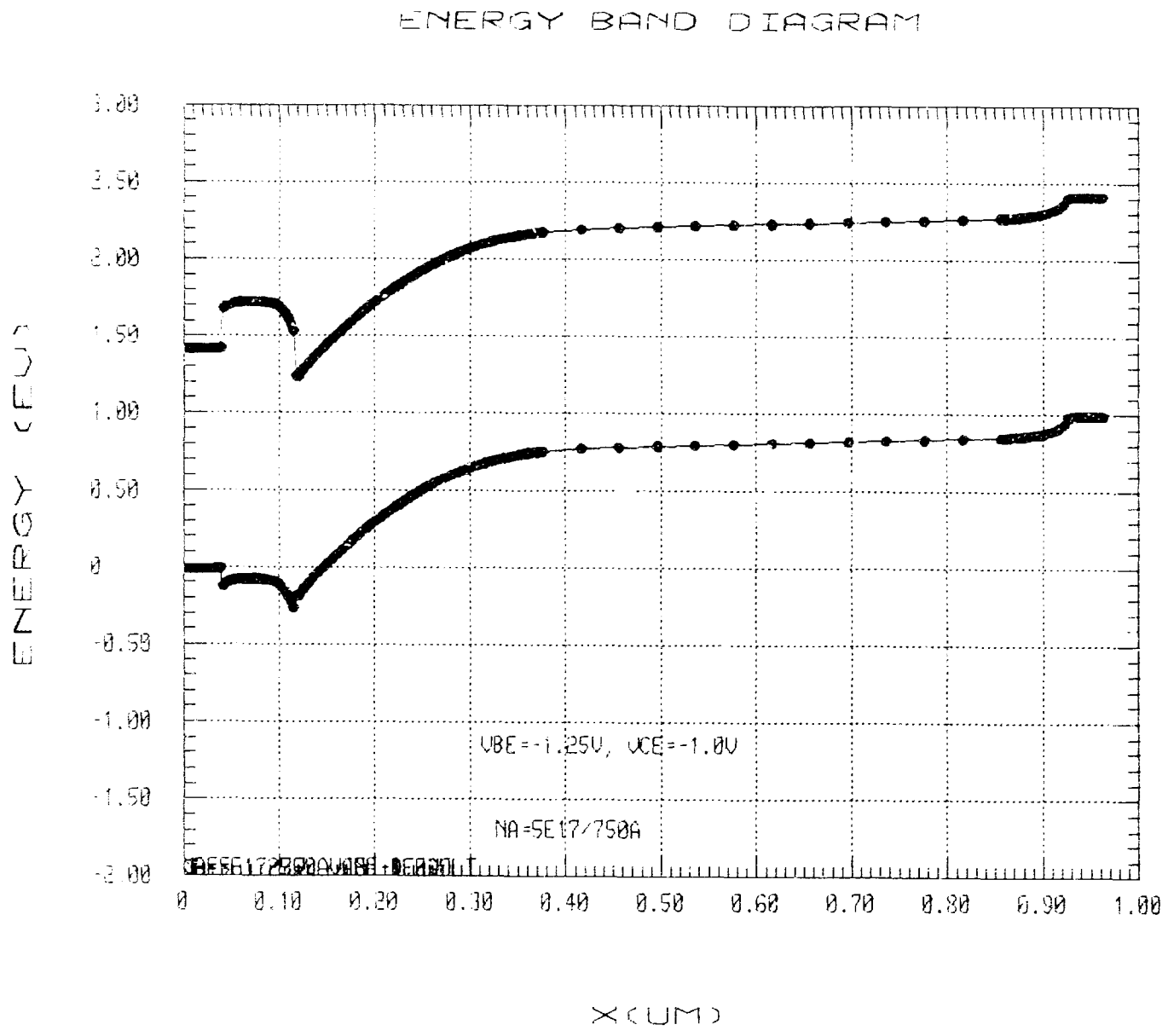


Figure 5.23 Band diagram for BICFET structure #G under bias

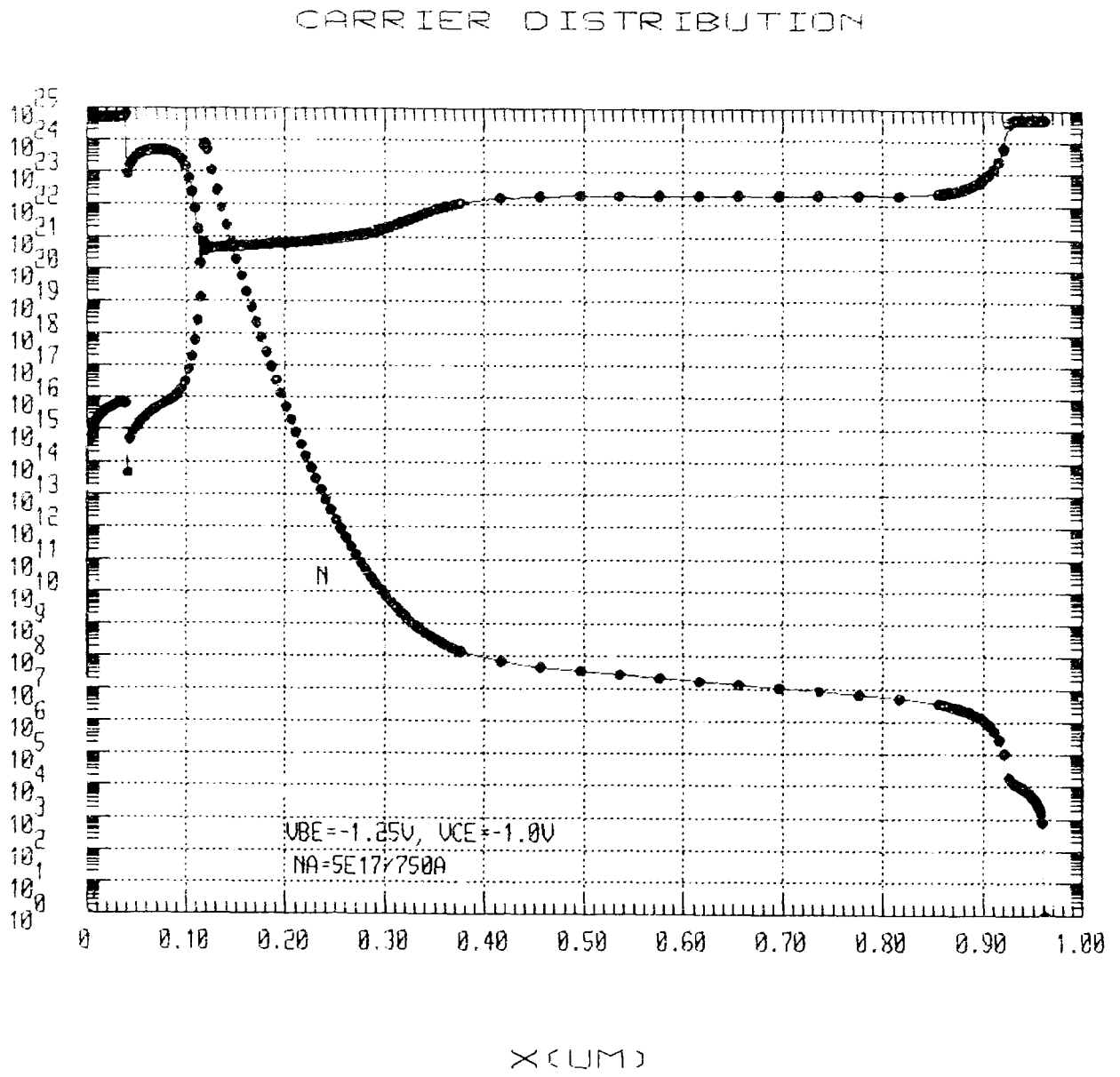


Figure 5.24 Carrier concentration distributions for BICFET structure #G under bias

5.4 BICFET MASK DESIGN

The BICFET device has a structure similar to that of a conventional bipolar transistor with the exception that the base contact has to make contact to an induced inversion layer. From the point of view of fabricating a BICFET, the processing steps and, therefore, the photomask requirements are also basically the same as for a bipolar transistor. Since the operation of the BICFET is totally dependent on the ability to create an inversion layer, test structures also need to be fabricated which would permit characterization of the inversion layer. With these requirements in mind, a mask set was designed for the purpose of fabricating discrete BICFET devices and material processing evaluation test structures. The mask set was designed so that devices could be fabricated on semi-insulating substrates although fabrication on conducting substrates could also be accommodated.

The mask set consists of six levels which are identified as follows:

1. Mesa (chemical, RIE or ion implant isolation)
2. Source A (base)
3. Emitter/Collector
4. Via
5. 2nd metal
6. Source B (base, same as A except receded from emitter by 2 μm)

Two source (base) masks were included so that ion implanatation doping for contacting the inversion layer could be carried out using source A and source metallization could be defined using source B. One mask is used for defining both the emitter and collector contacts and, therefore, mesa etching is required if devices are to be fabricated on semi-insulating substrates.

Two types of BICFET structure were included in the mask set. The first type, shown in Figure 5.25(a), requires one isolation step (mesa) and two metallization steps (collector/emitter and source) to complete the

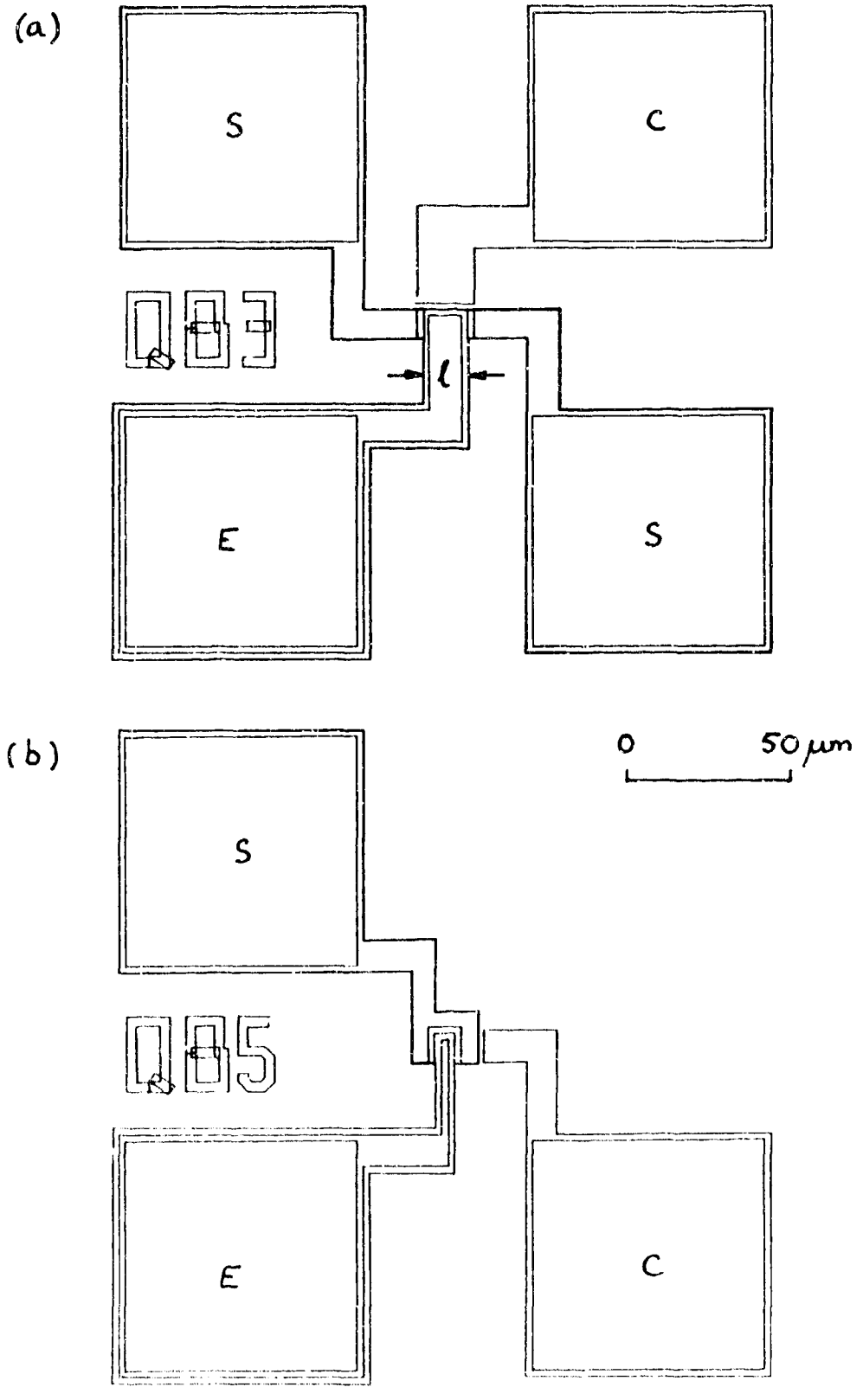


Figure 5.25 Schematic outlines of (a) dual source and (b) single source process evaluation BICFET structures which require three processing steps for completion

basic device structure. Since this device structure does not have a clearly defined inversion channel area, it is mainly intended as an evaluation vehicle for completion of the second type of device structure. A number of "effective" emitter area, type 1, devices were included with varying dual source spacing (l = 6, 9, 14, 24 μm) and width 9 μm. Since the source-emitter bias voltage is expected to appear in the region between the two source electrodes ("effective" emitter area), most of the emitter current should flow in this region, and, therefore, define the conducting channel. In addition to the dual source devices, which would be used for confirming the existence of an inversion layer, a single source device, shown in Figure 5.25 was also included. Since type one BICFETs have a large emitter area, due to the inclusion of the probe pad on the mesa, they could also be used for capacitance-voltage measurements under low emitter current conditions.

The second type of BICFET structure, shown in Figure 5.26(a), has mesa defined emitter and underlying inversion channel areas. In order to make contact with the smaller emitter and source areas, an insulating layer, e.g., Si_3N_4, etched via holes and a second level metallization are required. Emitter areas included in the mask design are 7x7, 9x9, 9x14, and 9x24 μm^2. Again, two sources were included to evaluate the inversion channel conductivity. One further BICFET device, with a single source, shown in Fig. 5.26(b) was also included in the mask design.

Since the emitter current of the BICFET is dependent on the biasing action of the laterally positioned source contact, some non-uniformity in the channel conductivity is possible. Therefore, a "potential probe" test structure, shown in Figure 5.27 was included in the mask design to measure the voltage distribution in the inversion layer. Here, a number of "voltage taps" were included along the channel between the two separate sources. This structure should be useful in determining what fraction of the channel is active and indicate how much the transistor action deviates from the one-dimensional theoretical predictions. The shape of the test structure is also appropriate for carrying out Hall measurements for determining the sheet resistance, carrier concentration and mobility of the inversion layer. This type of measurement is

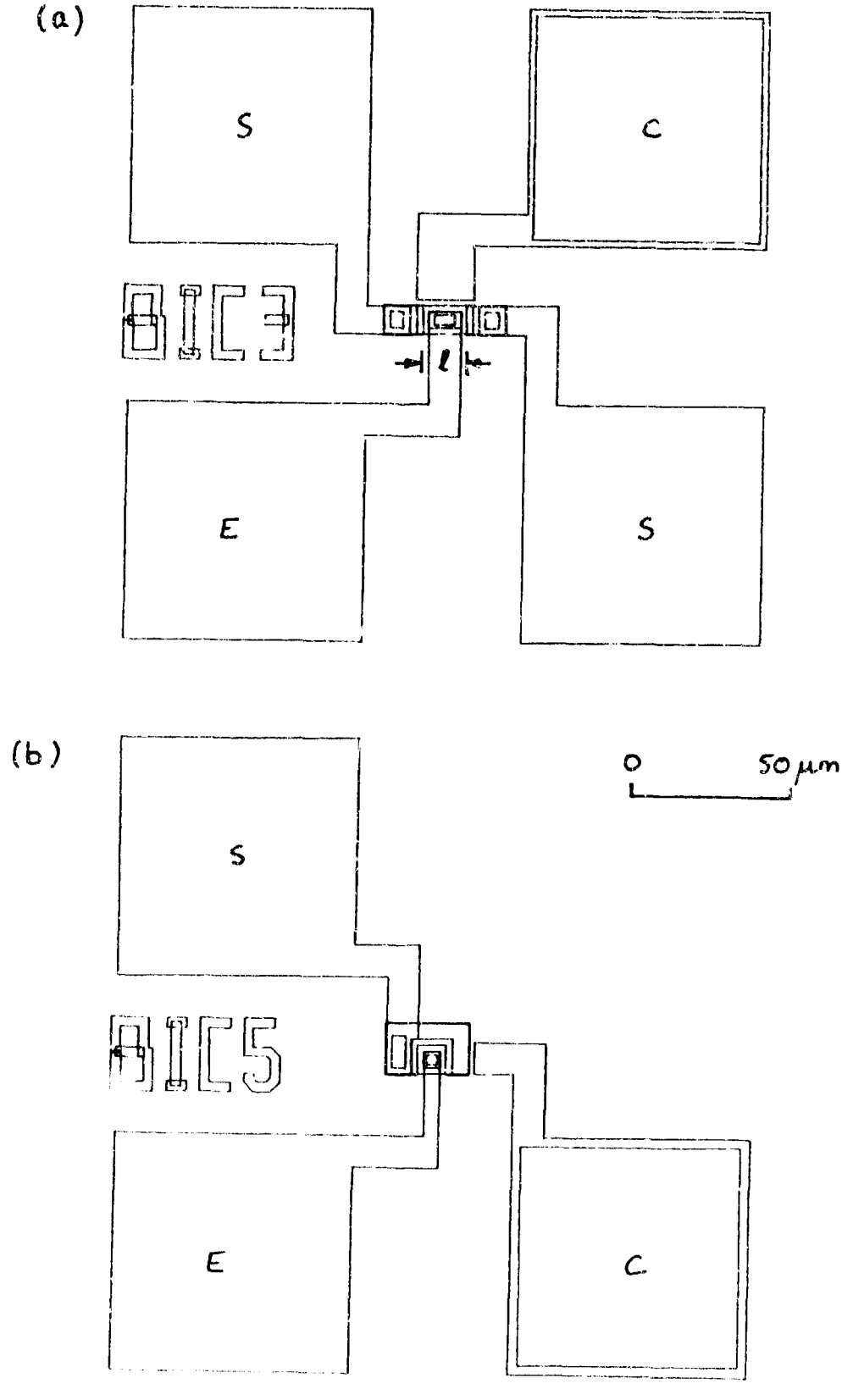


Figure 5.26 Schematic outlines of (a) dual source and (b) single source BICFET structures which require six processing steps for completion

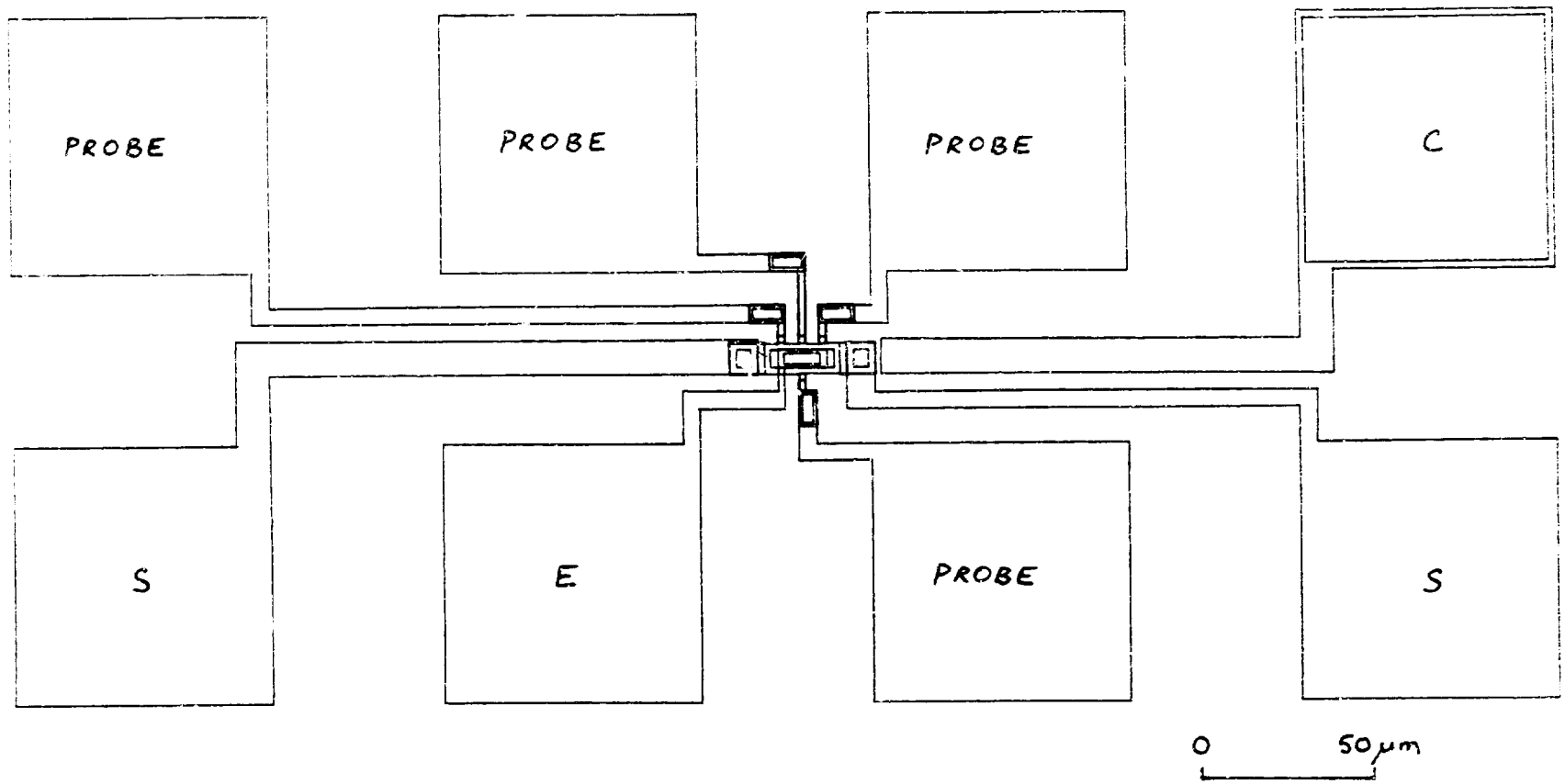


Figure 5.27 Schematic outline of the BICFET probe structure

strongly dependent on minimizing conduction paths parallel to the inversion layer and may not be possible during normal modes of transistor operation.

Shown in Figure 5.28 is a structure that would be used for measuring the source contact resistance to the inversion layer. Basically, the standard transmission line model (TLM) pattern was employed, except that in this case emitter contacts were located between the variable spacing source contacts. The source spacings are 7, 10, 13, 16, and 19 μm. The contact width is 20 μm. Measurement of the contact resistance to the inversion layer requires minimal leakage of source current to the emitter layer and uniform inversion layer resistivity between the adjacent sources. This requirement dictates that the transistor structure cannot be operated under normal bias conditions. If considerable emitter current is allowed to flow, then a suitable model for determining the contact resistance would have to be developed.

In addition to the BICFET devices, voltage probe and TLM pattern test structures were also added to the mask set to measure the emitter contact resistance and emitter layer sheet resistivity. Both TLM and Kelvin-Cross bridge structures can be used to measure contact resistance. In fact, the latter pattern is probably more appropriate due to the structural similarity with the BICFET. Kelvin-Cross contact areas included are 9, 25, 100 and 400 μm^2. One extended Kelvin-Cross bridge (six terminal) was also included to measure the end resistance in addition to specific contact resistance and sheet resistance of the material under the contact. Here, the contact area is 100 μm^2.

The composite die layout of the BICFET mask set is shown in Figure 5.29. The lower half of the layout was dedicated to BICFET device and test structure fabrication while the upper half was dedicated to the fabrication of MESFETs. Although, in general, the two processing technologies are incompatible, they share a number of masks and, therefore, could be accommodated on one mask set. In both sections, all of the devices and test structures were duplicated in orthogonal directions to test for directional performance characteristics.

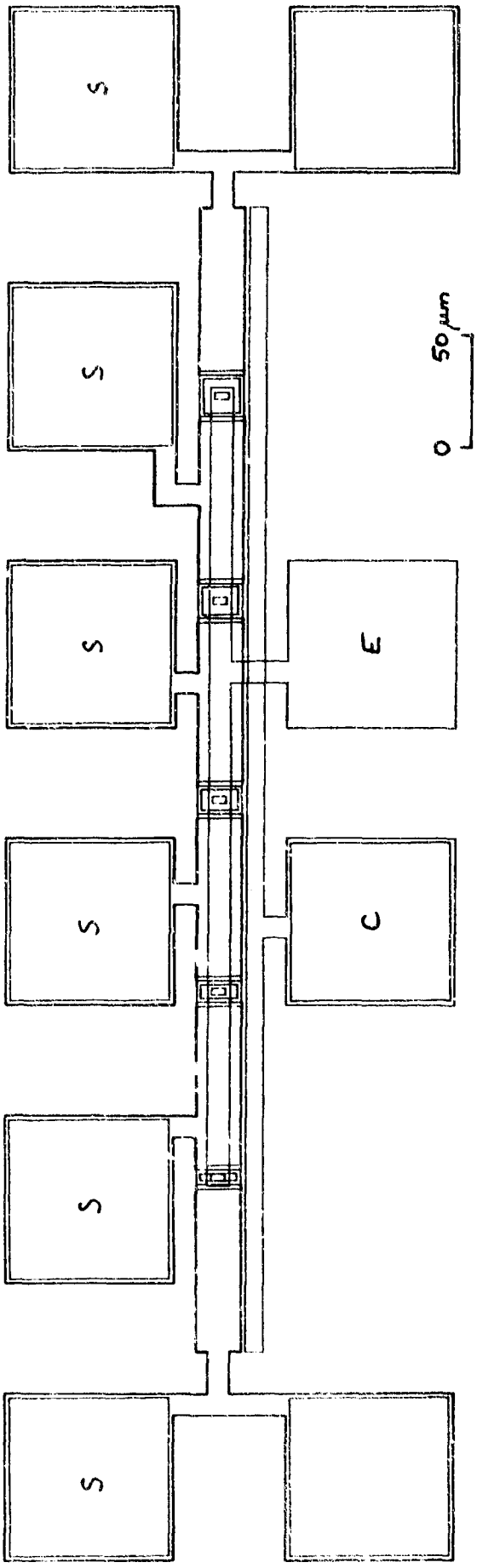


Figure 5.28 Schematic outline of the BICFET source contact resistance measurement TLM Pattern

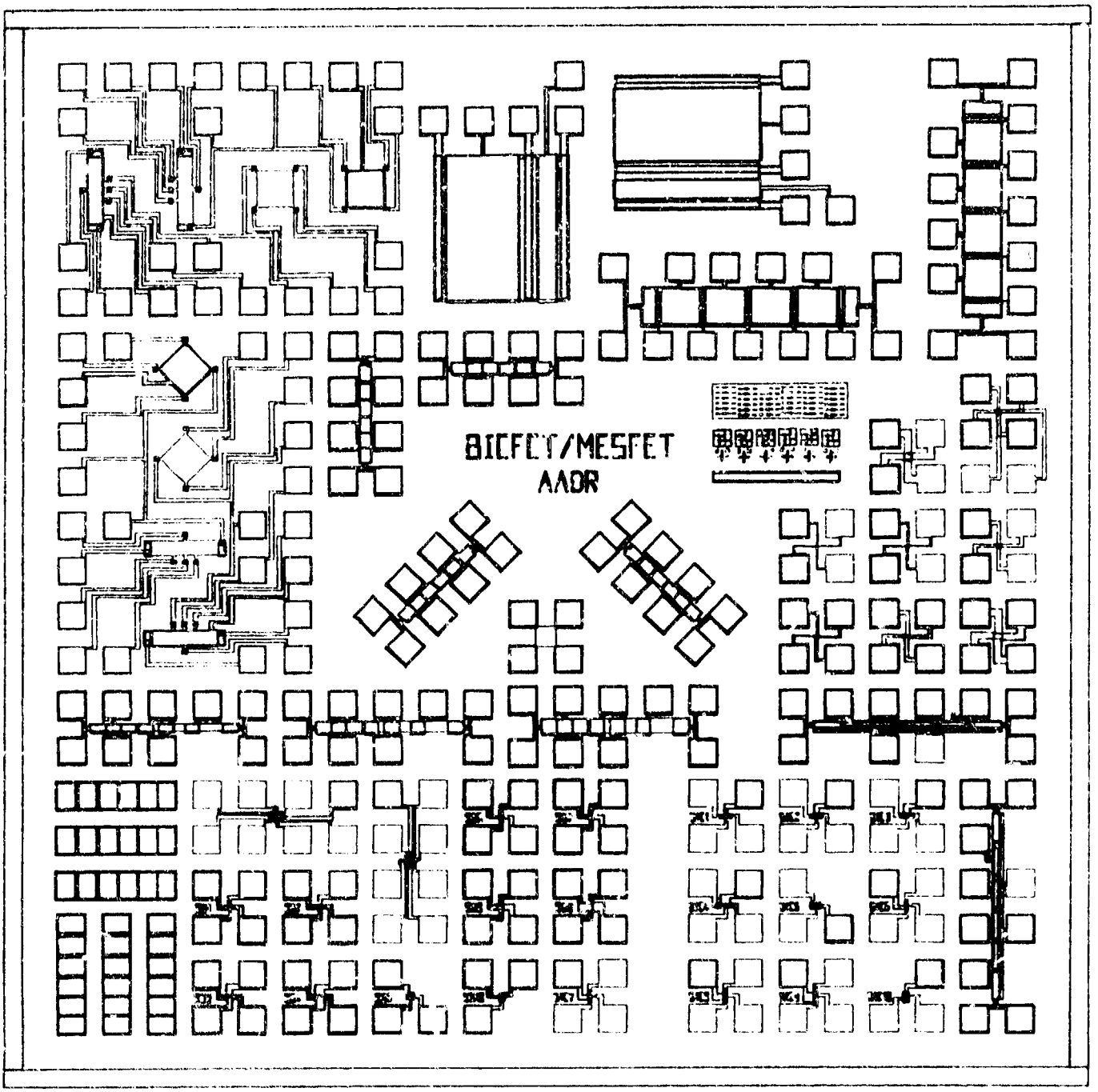


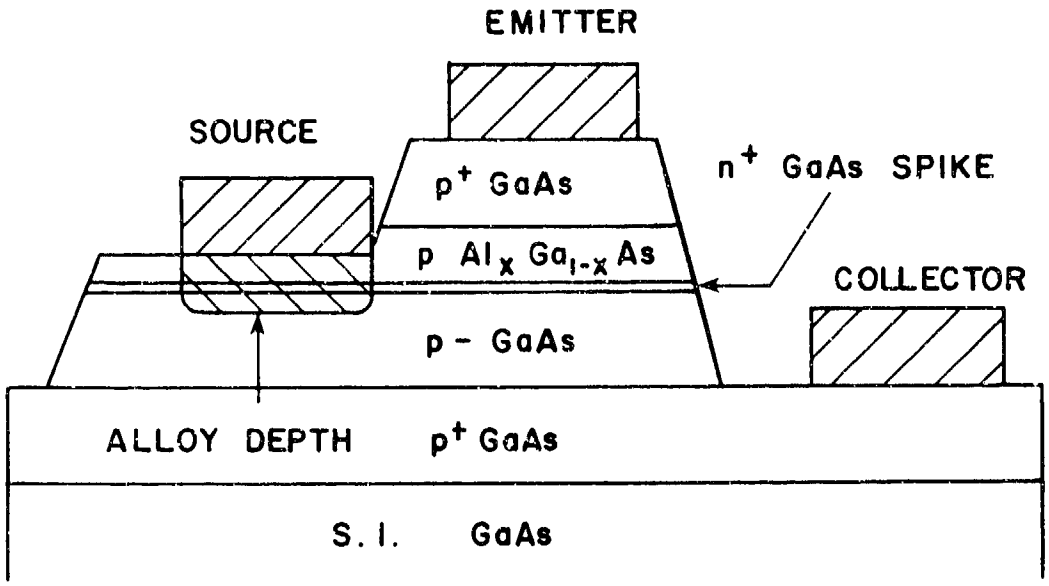
Figure 5.29 Composite die layout of the preliminary BICFET mask set

5.5 BICFET FABRICATION

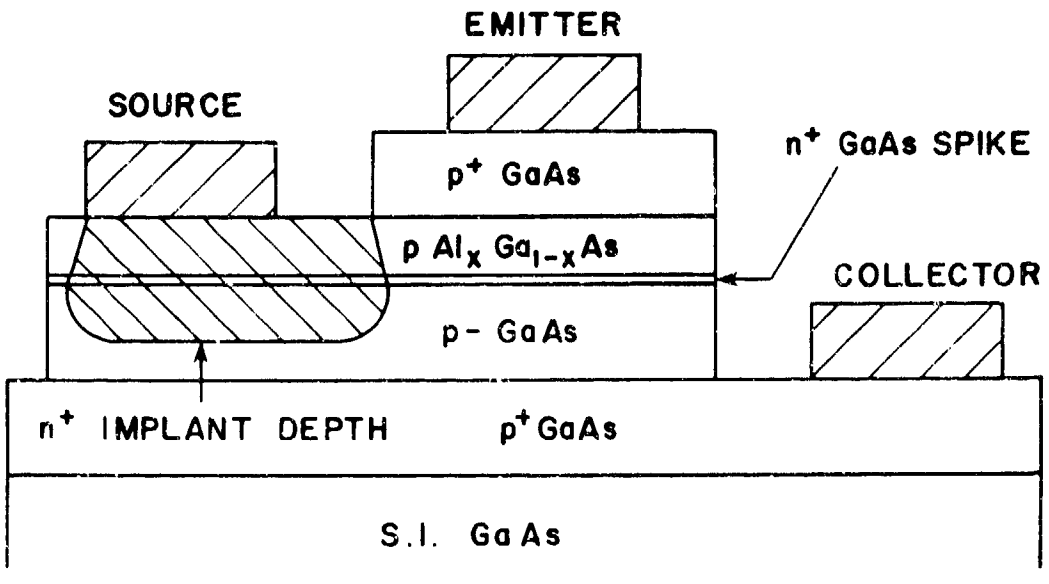
5.5.1 BICFET Structure

For AlAs mole fractions up tc $x = 0.45$, the $Al_xGa_{1-x}As$/GaAs system has a band structure appropriate for fabrication of n-channel BICFETs [18]. Since the BICFET has a structure similar to an n-channel Heterostructure Bipolar Transistor (HBT), with the exception of the base region, the fabrication processes are similar and can essentially use the same photolithography mask set design rules. The main difference in processing lies in the way contact is made to the source, which, in the case of the BICFET, is a very thin induced inversion layer existing only under the emitter area.

Two possible types of BICFET structure are shown in Figure 5.30. In both cases, the active device area is defined by chemical or Reactive Ion Etching (RIE) down to the p^+ GaAs buffer layer using standard photolithographic masking techniques. In BICFET (a) the next step is emitter and collector ohmic contact metallization, which can be carried out in one photolithographic lift off. The metallization most commonly used for making contact to p-type material is Au/Zn. The next step in the process is the delineation of the source contact. By using the same mask for recessing down to the wide-band gap AlGaAs layer and subsequent source metallization delineation, the source contact should be self-aligned with respect to the emitter. This recessing step can also, be carried out by RIE or wet chemical etching. In either case, selective etching of the GaAs with respect to AlGaAs is required. A further etch back of the AlGaAs may be necessary before deposition and alloying of the contact, although care should be taken to avoid etching beyond the n^+ GaAs spike layer. Location of the source metallization next to the emitter area is essential since a contact must be made to an inversion layer which will only be formed under the emitter. A gap between the source and emitter would essentially prevent any contact being made and the device would be unable to function. Alloying of both the emitter and source contacts can be effected by one temperature cycle. Conventional furnace annealing is probably the preferred choice for making ohmic



(a)



(b)

Figure 5.30 Schematic cross sections of n-channel BICFETs with (a) source contacts alloyed directly to the inversion layer and (b) ion implanted source contact layers

contact to the source, which in this device is an induced electron inversion layer. The metallization scheme most widely used for making ohmic contact to n-type GaAs is Au/Ge/Ni, and because we have found it to undergo considerable lateral and vertical penetration at the edge of contacts after conventional furnace annealing, it should be appropriate for this BICFET processing scheme [34]. A necessary requirement of this type of source contact is that the alloy penetrates all the way through the AlGaAs layer and that the p-type doping in the AlGaAs layer is electrically obscured. Completion of BICFET (a) is accomplished after deposition of an insulating layer e.g. Si_3N_4, via hole etching and second metal (interconnect) delineation.

In the second type of BICFET (structure - b), after the active layer defining mesa etch, the source region is recessed down to the AlGaAs layer. Again, either selective wet chemical or RIE etching can be used although the latter is preferred due to better uniformity and the ability to etch anisotropically. Using the same etch mask, a silicon dose is implanted in the source contact areas to a depth well beyond the AlGaAs layer. The dose should be sufficiently large to compensate the acceptor concentration in the AlGaAs layer after the annealing cycle. Rapid Thermal Annealing (RTA) should minimize diffusion of the silicon spike layer although, clearly, this is a processing step of some concern. Smearing of the thin (30 to 50 Å), highly doped spike layer would alter the band structure and may inhibit the ability of the structure to sustain an inversion layer. The RTA should be carried out under local arsenic overpressure rather than with dielectric passivation which, due to strain, may induce deleterious diffusion in the material structure. After the anneal cycle, BICFET (b) can be completed in the same manner as BICFET (a). However, in this case the alignment of the source contact immediately adjacent to the emitter area is no longer critical.

5.5.2 P-Type Ohmic Contacts

An essential requirement for obtaining optimum BICFET performance at high frequencies is low emitter, collector and source contact

resistances. Consequently, investigations were carried out on contact fabrication using the Au/Zn/Au metallization scheme. This scheme was adopted in order to obtain good adhesion, uniformity, and reproducible low resistance ohmic contacts. To limit the extent of Zn penetration into the epitaxial material, the thickness of the Zn layer was kept to a minimum.

In the investigations, 100 Å Au/200 Å Zn/2000 Å Au was deposited onto p-type GaAs ($p = 1 \times 10^{19}$ cm^{-3}, $t = 0.1$ μm) by resistance boat evaporation, and TLM contact patters were delineated using conventional photolithography. Annealing was carried out in a conventional furnace using a flowing N_2 ambient. The measured contact resistance as a function of anneal temperature is shown in Figure 5.31. The anneal cycle consisted of a ramp time of ~ 2 1/2 minutes followed by a peak temperature anneal time of 30 seconds. After annealing, the wafers were cooled in the

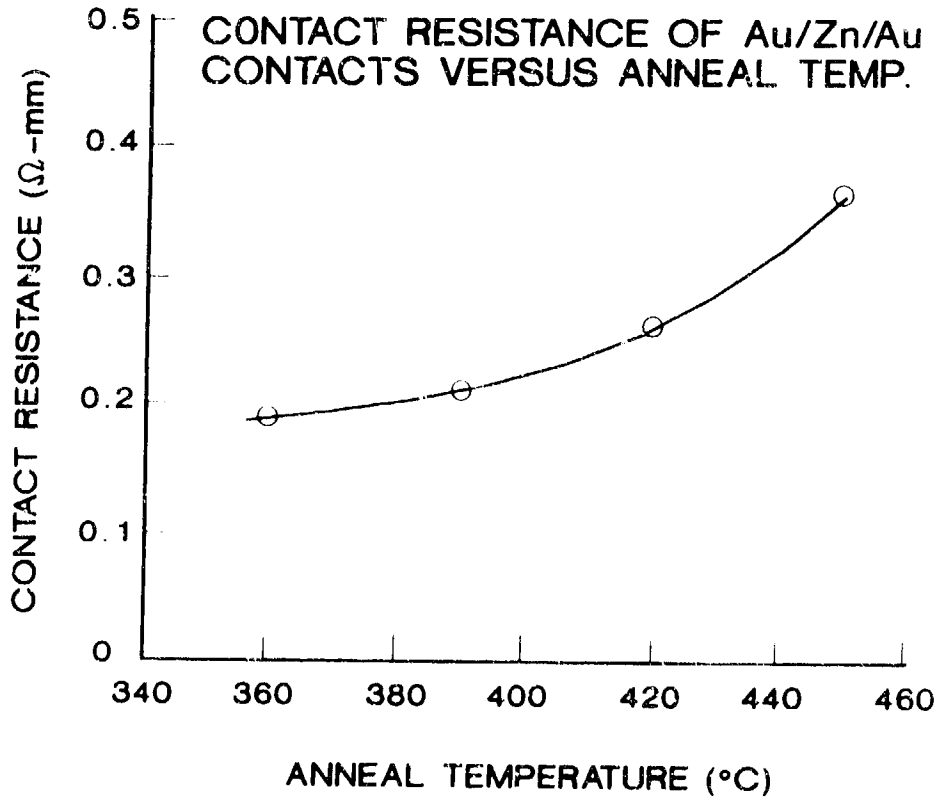


Figure 5.31 Contact resistance versus anneal temperature for Au/Zn/Au contacts to p^+ GaAs

cold zone of the furnace. For a 360°C anneal the average contact resistance measured 0.19 Ωmm with a corresponding specific contact resistance of 8.6×10^{-7} $\Omega\text{-cm}^2$. The Auger spectra, measured at AFWAL/AADR, of the contact metallization on GaAs before and after annealing at 420°C are shown in Figures 5.32 and 5.33, respectively. The As signal is omitted from the spectra for purposes of clarity. In the as deposited case, the residual Ga, Zn, and O_2 signals in the bulk of the 2000 Å Au layer correspond to background noise. In the annealed case, the Zn component has distributed itself through the Au metallization and falls off toward the surface. Penetration into the GaAs could not be resolved accurately since the zinc Auger peaks corresponded to strong Ga sub-peaks. As is normal for alloyed Au metallizations on GaAs, a large Ga and corresponding oxide peak were observed at the surface.

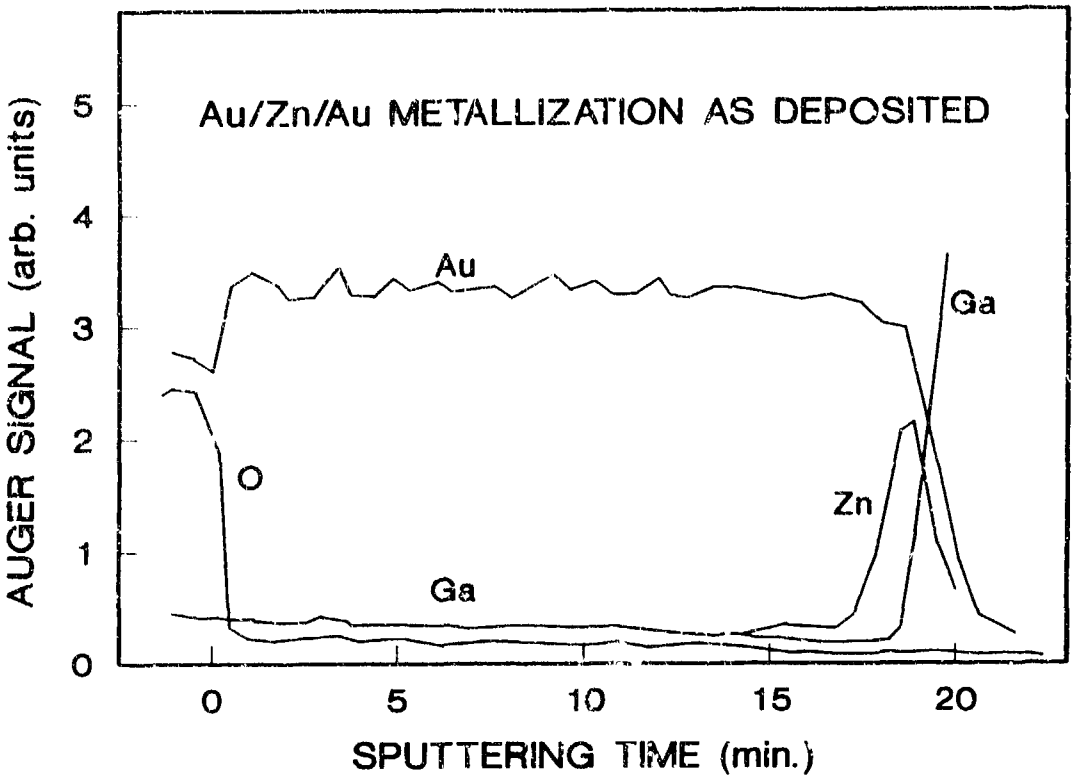


Figure 5.32 Auger profile of Au/Zn/Au contact to GaAs before annealing

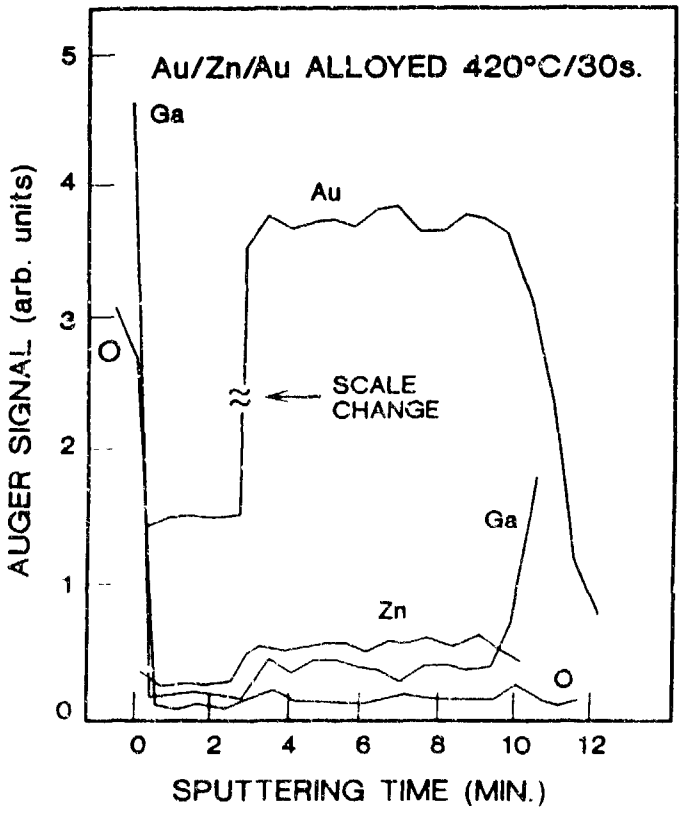


Figure 5.33 Auger profile of Au/Zn/Au contact to GaAs after annealing at 420°C for 30 second

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